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LNBUG #6.0 6500 DEVELOPMENT SYSTEM

AUTHOR - Larry Nicholson Cyan Engineering Grass Valley, CA (916) 273-6194

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TABLE OF CONTENTS

| | | Page |
|---|-------------|--|
| INTRODUCTION | | . 1 |
| BASIC COMMAND FORMAT . | | . 2 |
| COMMAND DESCRIPTIONS . RESET MODES LIST AND MODIFY MEMORY R Display User CP / List Memory SHFT / List One Location : Modify Memory . SHFT : Modify One Location K Macro Listing . | U Registers | · 2 · 3 · 3 · 3 · 4 · 4 · 5 · 5 |
| MACRO MEMORY OPERATORS M Move Memory Program Prom . Compare Memory V Verify Memory . # Fill Memory With Z Delete All Memo J Macro Command F | h Data Byte | . 6 . 6 . 6 . 6 . 7 . 7 |
| PATCHING COMMAND I Insert Patch . Listing and Sav | | • 8 • 8 |
| PROGRAM LOADING AND SA L Load Data From W Write Data to T " Suffix That Sel For Downloading U Upload Data to | VING | . 10 . 10 . 10 . 10 . 13 . 13 |
| KEY BUFFER OPERATORS . RUB Delete Last Ent LF Non-Destructive SP Delete Current ^H Backup One Addr ESC Delete and Esca CR Execute Current | ry | . 10 . 10 . 10 . 10 . 10 . 10 . 10 |
| FUNCTIONS FOR RUNNING G GO From Start O P Proceed From Cu S Set Single Step T Set Trace Mode N Set Number of S B Set Breakpoints ^C Re-enter Monito @ Run Subroutine | PROGRAMS | . 11 . 11 . 11 . 11 . 11 . 11 . 11 . 12 . 11 |

÷

| SUFFIXES .< | 2 2 2 |
|--|-------------|
| RELOCATION REGISTER | 2 2 2 |
| TERMINAL CONTROL | 2 |
| H Set Hard Copy Mode | .2 |
| PDP-11 COMMUNICATIONS. . | |
| APPENDIX Assembler/Disassembler Format | |

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LNBUG 6500 DEVELOPMENT MONITOR

INTRODUCTION: The MCS6500 Development Monitor is a comprehensive debug package including complete list and modify commands, mini-assembler/disassembler, disc and tape communications, stepping, trace, and breakpoint capabilities, and other useful memory manipulation commands. The program is designed to run on an S-100 type computer utilizing an Atari trace memory interface board with a video or hard copy terminal.

To run the monitor, the system must be configured as follows:

1 - Atari GVA-25Ø3 CPU card (or Coleen wire wrap CPU)

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- 1 Dynabyte 16K RAM card
- 1 Cromemco 16K ROM card
- 1 Atari GVA-25Ø4 Trace Memory Interface Card

Make sure to set switches as specified on sheet labeled "DEVELOPMENT SYSTEM SWITCHES." A copy of this is included at the back of this manual.

With the BOOTSTRAP switch on, the monitor will be entered upon reset, starting at location $6\emptyset\emptyset\emptyset$ (GVA-25 \emptyset 3 only).

If reset is desired to clear vectors and reset all monitor cells, a carriage return should be the first character entered. A "Cool" Reset will clear everything except patches and breakpoints. (Type "C".) A "W" causes a warm reset and clears nothing. The monitor will echo

"NOW ENTERING LNBUG #X"

to indicate the entry to the monitor and the version being used.

After a "Cold" reset, the user must select the control set for the terminal being used:

Type "H" <CR> for a hard copy terminal. For Lear Siegler, type nothing.

The monitor is now ready for operation.

Note: See Appendix on Interrupt Handling for Colleen ROM O.S.

BASIC COMMAND FORMAT:

Commands to the monitor are entered in a line at a time in the deferred mode or with a single keystroke in the immediate mode.

The command and the optional suffix are always entered in after necessary address and data entries.

Examples:

Format

Example

| Command Suffix | DX |
|--------------------------|-----------------|
| Adr Command Suffix | løøø/Q |
| Adrl.Adr2 Command Suffix | 1ØØØ.11ØØ/Q |
| Adrl.Adr2, Data Command | løøø.lløø,øø# |
| Adrl.Adr2, Adr3 Command | 1ØØØ.11ØØ,1ØØ3M |

"Adrl.Adr2" indicates start and stop addresses. "Adr3" indicates destination address, "Suffix" is always optional. "Deferred" commands are line oriented and all key entries are stored in a buffer until <CR> is hit. The buffer can be modified prior to execution using various key buffer operators.

COMMAND DESCRIPTIONS:

The following descriptions are organized into the following groups:

List and Modify Memory Macro Memory Operators (Move, Verify, etc.) Patching Command Program Loading and Saving Key Buffer Operators Functions for Running Programs Suffixes Relocation Register Terminal Control PDP-11 Communications In the following descriptions, Mode "D" is the

deferred mode and "I" is the immediate mode. (See descriptions above.) All values are in hexidecimal.

Reset Modes

- CR Cold reset clears all breakpoints, patches, vectors, step-mode, hardware, etc.
- Cool reset clears everything except break-С points, patches, "K" macros, and "J" macros. W - Warm reset clears hardware only.

LIST AND MODIFY:

| Command | Mode | Description |
|---------|------|--|
| R | I | Display user CPU registers. |
| | | EX: User types- R |
| | | Monitor prints: |
| | | PC=2000 P=00 A=01 X=FF Y=FF S=EA |
| / | D | List memory from start to stop address. Or, if start address only is specified, all locations up to the next address increment of sixteen will be listed. |
| | | EX: User types- 1000.1008/ (echoed) |
| | | Monitor prints after return: |
| | | |
| | | EX2: User types- 100A/ (echoed) |
| | | Monitor prints after return: |
| | | Ø 1 2 3 4 5 6 7 8 9 A B C D E F 1ØØA = B9Ø1 21 C9ØØ DØ |
| | | EX3: User types- 2000.2006/Q (echoed) |
| | | Monitor prints after return: |
| | | 2000 LDA I,0FF 2002 STA Z,10 2004 DEX 2005 BNE 2028 |
| / | I | When no address is specified, list the next sixteen locations starting from the last list address plus one. Allows convenient continuous listing. |
| | * | EX: User types- / (not echoed) |
| | | Monitor prints: |
| | | 1Ø1Ø = AA 99 24 32 7D A9 CØ ØD (etc.) |

LIST AND MODIFY (continued)

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| Command | Mode | Description |
|---------|---------------------------------|--|
| SHFT / | I | List one location. |
| | | EX: $1000/$ (echoed) |
| | | Monitor reprints line on shift /: |
| | | $1\emptyset\emptyset\emptyset = A9$ |
| | | A repeat of just the shift / prints: |
| | | $1\emptyset\emptyset\emptyset = A9$ again |
| | | (This is useful for reading PIA ports) |
| : | D | Modify memory. Opens memory for modification starting at specified address. Memory is not actually modified until carriage return is hit or until address passes over an increment of sixteen. (Automatic carriage return for con- tinuous entry.) All key buffer operators can be used. (Rub, escape, etc.) |
| | EX1: User types- 1000: (echoed) | |
| | | Monitor prints: |
| | | Ø 1 2 3 4 5 6 7 8 9 A B C D E 1ØØØ = |
| | | The cursor is then positioned under " g " waiting |

for a user entry.

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EX2: User types- l g g g: (echoed)

Monitor prints:

1000:Q

The monitor is now waiting for the user to enter in mnemonics.

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TIDI WUD WODILI (COULTURED)

Command Mode Description

:

Κ

I Modify memory starting at start of prior listing. Or, modify user CPU registers if "R" command preceded ":" command. All other characteristics are identical to ":" in the deferred mode.

EX: User types- 1000/

Monitor prints locations $1\emptyset\emptyset\emptyset-1\emptyset\emptysetF$ as shown above. User then types : (not echoed)

Monitor prints:

1000:

The monitor is now waiting for user entry. Note: If listing was made using the immediate mode "/", the beginning of the current line will be opened for modification.

SHFT: I <u>Modify one location</u>. Immediate modification of one location.

EX: User types- SHFT:

Monitor prints:

løøø:

-

Only this one location will be modified and address location pointer is not incremented.

D Macro Listing Command. A macro listing command used during trace or under user control. Up to six single locations or lists (of any length) can be specified and then listed either during breakpoint/step operation or when "K (CR) " is specified. To set these, specify: Adrl.Adr2 - List, Adrl - Single location. Separate with commas, and end line with "K (CR)." Any number of entries (up to six) are allowable and can be in any order. The "X" suffix clears the "K" directory.

EX: User types- ØØ.ØF, 4Ø94, 4Ø21K

When a breakpoint occurs in a user program, or if the user types in "K < CR> ", the monitor will print:

Note that if trace mode is set, the listing will be made after every breakpoint, whereas, if the trace mode is not set, the listing will be made after passing through the breakpoints "N" times as set by the "N" command.

MACRO MEMORY OPERATORS

Command Mode Description

M D <u>Move memory</u> from start address to stop address to destination address. Accounts for direction of move to prevent memory destruction in overlapping moves.

EX: User types - 1000, 10FF, 1003M

Monitor then moves block up three bytes.

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D Program 27Ø8 EPROM's using Byte-Saver board. Specify source start and stop addresses and destination address (Byte-Saver address). Any number of bytes can be programmed at a time without timing problems as the program always maintains at least a "1K Duty Cycle" to prevent damage to the PROM.

EX: User types- 1000.13FF,8000!

Programs RAM area $1\emptyset\emptyset\emptyset$ to 13FF to the PROM located at $8\emptyset\emptyset\emptyset$.

Monitor then prints:

PROM AREA O.K. IS PROGRAMMER UNPROTECTED & READY?

The user then types either "Y" for yes or "N" for no. Yes starts the programmer, no returns control to the monitor.

Note: This program must be downloaded first. The download sets all vectors needed. (BYTSVN.MC

D Compare memory. Compare one block of memory with another. Specify start and stop addresses of one block and start address of block to be checked ()

> For example, see move instruction and verify ininstruction.

V D Verify proper memory operation by writing "55" at "AA" to locations, while saving current contents non-destructive checking. Specify start and stop addresses.

EX: User types- 2000.3000V

Monitor prints:

First error $24\emptyset\emptyset$ Total errors = $1\emptyset24$

- 6 -

MACRO MEMORY OPERATORS (continued)

| Command | Mode | Description |
|---------|------|--|
| # | D | Fill memory with specified data byte, starting at Adrl and ending at Adr2. |
| | | EX: $1000.1FFF,000$ will set locations 1000 to $1FFF$ with "00." |

J D or I <u>Macro Command Files</u>. Up to eight (Ø-7) separate lines of commands can be stored and later recalled without having to re-enter all addresses, data, etc. This is useful for periodically listing a section of memory, setting breakpoints, etc.

Setup Macro Command:

EX: 1000.10FF/3J - Sets macro command file #3 to 1000.10FF/.

Execute Macro Command:

EX1: 3J - Execute command set up in above example.

EX2: J - Immediate command to execute contents in file #Ø.

List Macro Command:

EX: \emptyset/J - List zero macro command file.

Delete Macro Command:

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EX: 7JX - Deletes macro command file #7.

PATCHING COMMAND

2, TSX

Command Mode

Description

I

D

Insert patch in program. Allows user to specify an address in the program under development and insert instructions at this address without affecting the rest of the program. The monitor actually places the patched code in a "Patch Area" and inserts a "BRK" at the user program address upon starting the program. Utilizing a "Patch Directory," the monitor is able to vector the user program to the proper patch in the patch area upon encountering a "BRK." The patch has already been constructed automatically to jump back to the user program.

EX:

User Program 1999 LDA 1,99 1992 STA 2X,93 1994 DEX 1995 BNE 1999

Insert "DEY" at 1002. Patch area: 40A6 DEY 40A7 STA ZX,03 Added automatically 40A9 JMP 1004 by patch program

Or, insert "BPL 1010" at 1005 Patch area: 40C6 BMI 40CB 40C8 JMP 1010 This structure automatically 40CB BEQ 40D0 constructed by patch program 40CD JMP 1000 40D0 JMP 1007

Note that upon return to monitor, all "BRK" instructions are replaced with the original instruction making the patch transparent upon listing.

Eight blocks of 32 bytes each are maintained in the patch area. Thus, a maximum of eight patches can be made. If a patch consumes more than 32 bytes, it will automatically link itself to the next patch area block provided the block is free.

A patch is specified by entering in the address, the desired patch number (optional - automatically finds available patch), the "I" command, and a carriage return. The desired instructions are then entered in mnemonics a line at a time. Two carriage returns in a row will terminate the patch PATCHING COMMAND (continued)

Command Mode Description

The patch is effectively placed just prior to the address specified. Note that this type of patch consumes an average of 100-200 processor cycles and should not be used in time critical operations.

> EX: Ø,4IX deletes patch #4 "IX" deletes all patches

LISTING & SAVING PATCHES

"I" lists patch directory for reference use.

To save patches and breakpoints, write locations CØ64-CØA5 to the disc or tape. Note that this will also store the trace mode, relocation register, and step counter. DO NOT RECORD this section while in step mode. Always load this section before setting step mode.

PATCH & BRKPNT WARNING

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If a location that is a patch is modified, that patch will be deleted from the patch directory. But, if the location is changed to a $\emptyset\emptyset$, the old patch code will be replaced and the patch maintained, even though the program will not run correctly. Care should be taken when modifying patched code. References to patches here also apply to breakpoints.

PROGRAM LOADING/SAVING

Command Mode Description

- L D Loads data from terminal or auxiliary port in the standard MOS Technology LOAD format. Returns control to monitor upon receipt of an ASCII DC3 (Control X-Off). No address is specified. Note that tapes made with this monitor contain the "L," <CR> and DC3, so loading is done by simply turning on the tape. Echoes on terminal if trace mode is set.
 - W D Write hex to terminal or to auxiliary port in standard MOS Technology format. Specify start and stop addresses in the usual fashion. Note that an "L," <CR> and DC3 are transmitted at the proper times to allow simple reloading.
 - " Suffix Select auxiliary port load or write. Add as a standard suffix to the L or W commands. See "PDP-11 Communications" for uploading and downloading from PDP-11.

KEY BUFFER OPERATORS

- RUB I <u>Delete Last Entry</u>. Rubout erase last entry. On Lear Siegler, underscore is equivalent; i.e., shift is not required.
- Line Feed I <u>Non-Destructive Advance</u>. Advance one address or one instruction (in mnemonics mode) if first entry of line, or one character in any other mode. Does not affect contents of buffer or memory. This should be used only to skip a previous entry. Space should be used initially if skips are desired.
- Space I Delete Current Entry and Advance. Erase previous key entry and advance one address if modifying memory in hex mode. Otherwise, print non-functioning space character.
- Backspace I Back Up One Address.

(Control H)

Escape I Delete and Escape Current Line.

CR I Execute Current Line.

FUNCTIONS FOR RUNNING PROGRAMS

| Command | Mode | Desc | rip | tion |
|---------|------|------|-----|------|
| | | | | |

G

T

N

B

D <u>Go From Start of Program</u>. "GO" starting either at specified address or at address specified in previous GO command if no address is specified, (for restarting program).

EX: First Pass: 1000G

 Starts program at 1000. Thereafter, typing only a "G (CR) " will start program at 1000.
 Suffix Attach to "G" command to run a subroutine. Note: All user registers valid except PC.
 P I Proceed From Current Program Address. (Proceed from BREAKPOINT, SINGLE STEP, Control C, etc.

- 5 D Set single step mode (Use SX to reset to continuous mode.) NOTE: If Coleen ROM O.S. is used, LNBUG5 address prom must be used also, see Appendix on Interrupt Handling.
 - D Set trace mode (use TX to reset). Lists breakpoint #, CPU registers, next instructions, and any memory locations as specified in K command upon breakpoints or single step. Also used to specify an echo upon loading programs via the terminal (See "L" command.)
 - D Set Number of Steps or Breakpoints. Set number of times through breakpoints or single step before tracing and returning to monitor. Specify any hex number up to "FF." Note that "ØN" will run continuously. Specifying just N with no number defaults to Ø1. EX: "IØN <CR> " will cause 16 breakpoints or steps to run before stopping.
 D Set Breakpoints, List Breakpoints. Specify
 - as: ADR,#B where # is the breakpoint number (1-8). Specifying Ø,#BX will delete that breakpoint. BX deletes all breakpoints. "B" only lists breakpoint directory.
 - EX: User types- 1004,3B

Run Program (trace mode set, $N=\emptyset 2$).

Monitor prints:

#3 PC=1 \emptyset Ø4 A= \emptyset 1 X=FF Y= \emptyset Ø S=FA BNE 1 \emptyset ØØ #3 PC=1 \emptyset Ø4 A= \emptyset 1 Y=FE Y= \emptyset Ø S=FA BNE 1 \emptyset ØØ

CAUTION: See warning in "I" instruction about modifying location specified as a breakpoint or patch.

FUNCTIONS FOR RUNNING PROGRAMS (continued)

Control C I Reenter Monitor From User Program. Returns control to monitor while running a user's program. Uses IRQ interrupt processing. Will not function if vectors are changed or interrupt flag is set.

SUFFIXES

- Q Set Mnemonics Mode. Used to cause monitor to speak and listen in mnemonics rather than hexidecimal. Applies only to "/" and ":" commands. This is a single pass assembler and maintains no symbol handling capabilities. "I" command assumes mnemonic mode. For examples see "/" and ":" commands.
- X Delete suffix used to reset trace and single step and delete breakpoints, patches, terminal modes (H & D), and K listing. Note that using only a command and the X suffix deletes all breakpoints, patches, or K listings.

RELOCATION REGISTER

- Y D Set relocation register address. For use with relocatable program sections (CSECT).
- Y Suffix Add Relocation Register to Address. Used as a suffix to any address that is a relative address and must have the relocation register added to it. EX:
 - 1.) 1000Y <CR> sets relocation register at 1000.
 - 2.) Ø1A2Y/<CR> lists locations 11A2 thru 11AF on screen.

TERMINAL CONTROL

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D Set Hard Copy Mode. Sets monitor to use hard copy control set as well as delaying carriage returns and not double printing for such operations as rubout.

Upon cold reset, the monitor assumes the Lear Siegler video terminal control set. Use "X" suffix to reset hard copy. U

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- \$ D Enter bidirectional communications between terminal and PDP-11 host computer. Note: Since no buffering is used, the LNBUG terminal should always run faster than the computer baud rate. Since trace memories require 19,200 baud, this should not be a problem.
- ^ D I <u>Return to LNBUG</u> monitor from "\$." (All other characters are passed on to the PDP-11.)
 - D Upload from LNBUG to PDP-11. Specify start address and stop address in standard format. User will now be talking directly to the PDP-11

EX: 1000.12FFU (CR) (user enters)

.TSX Ver 3 (PDP-11 echoes) 12-Mar-79

.UPLOAD filnam.ext (User enters) \$ <CR> <CR> *Now entering LNBUG #4 (LNBUG re-entered)

Download to LNBUG from PDP-11.

- EX:T < CR>(User enters)\$ <CR>(User enters)
- .TSX Ver 3 (PDP-11 echoes) 12-Mar-79
- .DLOAD filnament (User enters)
- ;182000 (Data) (PDP-11 sends data)

Now entering LNBUG #4 (Back to LNBUG)

Note: "Upload" allows only 4.5 KB (approx.) of loading per file unless upload command file is modified (TSX).

APPENDIX

ASSEMBLER/DISASSEMBLER FORMAT

The format for the assembler is identical to that of the Atari MAC65 format (excluding symbols). This assembler is a 6500 adaptation of the RT-11 MACRO, written by Dave Sheppard of Coin-Op Engineering.

EX:

Mnemonic Address Operand Mode Comma Separator

Note that the development assembler does not recognize symbols and all operands must be in hexidecimal. The "Y" relocation suffix can always be specified. Branch instruction operands are specified as the absolute (or relocatable "Y") address. The offset address is then calculated from this address.

If an error is detected, the assembler prints the error message and then returns the cursor to the beginning of the line for re-entry of that line.

To terminate assembly, hit carriage return without entering any other keys (blank line).

Address Mode Specification -

| (none) | - | Relative, Implied, Accumulator, | 01 |
|--------|---|---------------------------------|----|
| | | Absolute (Default). | |
| I | - | Immediate | |
| Α | - | Absolute | |
| Z | - | Zero Page | |
| NX | + | (Indirect,X) | |
| NY | - | (Indirect),Y | |
| ZX | - | Zero Page,X | |
| AX | - | Absolute, X | |
| AY | - | Absolute,Y | |
| N | - | Indirect | |
| ΖY | - | Zero Page,Y | |
| | | | |



NEW COLLEEN ADDRESS MAP August 23, 1979

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| RAM | Ø-5FFF |
|-------------|----------------|
| ROM | 6ØØØ-7FFF |
| RAM | 8ØØØ-Bfff |
| LNBUG RAM | CØØØ-C7FF |
| PROM SOCKET | C8ØØ-CFFF |
| DØØØ | CTIA |
| Dløø | VACANT-ON CARD |
| D2ØØ | POKEY |
| D3ØØ | PIA |
| D4ØØ | ANTIC |
| D5ØØ | EXTERNAL |
| D6ØØ | S100 IO |
| Ø Ø Ø | ACIA'S |
| D8ØØ-Dfff | ON BOARD RAM |
| EØØØ-FFFF | RAM/O.S. ROM |
| | |

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MONITOR SUBROUTINES

The following subroutines can be called by a user's program for terminal communications and other useful functions. To use, assemble the file MONSBR.MAC with the user program. It is a set of equates that call the routines. (File on G.V. System Disc).

Juli Story Black

1 3 . . . P.

The following describes the routines:

| GETKEY=6ØØØ | Get character from terminal |
|----------------|--|
| GETHX=6ØØ3 | Get two ASCII characters & compact to hex byte |
| PRINT=6ØØ6 | Print ASCII character on terminal |
| HXPRNT = 6009 | Print hex byte in two ASCII characters |
| SP=6ØØC | Print space |
| BAKSP=600F | Print backspace |
| RETURN = 6012 | Carriage return line feed w/delay for hard copy |
| LINEED=6015 | Linefeed only |
| HTAB = 6018 | Tabulate non-destructively N spaces |
| KEYHND=601B | Master keyboard handler has rubout advance. |
| | back up etc Characters are put in "buff" |
| | starting at logation BUFFALF and working back- |
| | wards to BUFF The V register is returned with |
| | a pointor where PUEELY points at the last entry |
| | a pointer where burrth points at the last entry. |
| | To retrieve additional characters, increment X |
| | until X=1F. A maximum of 32 characters can be |
| | entered into builer. The 33rd entry will cause |
| | a return with the zero flag not set. |
| LSTHEX=6Ø1E | List hex from start to stop addresses. |
| | Set the following locations: |
| | 82,8A - Start ADL |
| | 83,8B - Start ADH |
| | 86 - Stop ADL |
| | 87 - Stop ADH |
| | Note that pseudo locations are printed for ØØ-Ø3 |
| LSTHED=6Ø21 | Same as LSTHEX except adds header to printout |
| LSTQ=6Ø24 | List mnemonics from start to stop. Set para- |
| | meters as shown above. |
| DISASM=6Ø27 | Print current instruction in mnemonics. Specify |
| | only start address parameters above. |
| WARMST=6Ø2A | Monitor re-entry point |
| TDELAY=602D | Carriage return delay (10 null characters) |
| HEXX = 6Ø3Ø | Converts ASCII character to LSD hex |
| KEYSTATUS= | |
| CØB2 | 6850 status save cell for processing user key- |
| | board interrupts (6850 status register is not |
| | valid if a key has caused an IRO int). |
| BUFF=CØ3E | Key huffer |
| USTROL= $C2B8$ | User IRO vector under Coleen ROM O S |
| IISTROH=C2BQ | ODEL INV VECTOL UNGEL COIEEN NON 0.0. |
| ODINGH-CID9 | |
| HIROL=FFF8 | User IRO vector without Coleen ROM O S |
| HIROH=FFF0 | USER ING VECTOR WICHDAL COTECH NON 0.0. |
| HTRAH-LII 2 | |

DEVELOPMENT SYSTEM SWITCHES

z-2 BOX - RESET: POC to complete system.

Set baud to monitor terminal. Set one TMI - TERM. (1) switch only for desired rate. Set baud rate for 2nd serial channel. AUX A15-8 Address decode of 2 serial channels. Set for D7 negative logic-A15 A14 A13 A12 COLEEN ALC A9 A8 POLARITY Up for Aux port connection to PDP-11 (Term.) Down for Aux port connection to term. (Comp., PROCESSOR (GVA-25Ø3 Only) RESET Local reset to processor and associated TMI Selects processor clock 1 MHZ 2 MHZ Use only one switch at a time. (ON=SELECT) EXT CLK JOLT / PROM Selects one of two address decode maps, (ON=JOLT, OFF=LNBUG) Enables power-on remapping of 7FFF to FFFF. BOOTSTRAP (Force Al5 on reset if switch is on) BUS DISC. Enables processor to system buss vs. stand alone (ON=normal, OFF=disconnect). W.D. DISABLE Kills a .1 s hardware watchdog reset. (ON=DISABLE WATCHDOG) W.D., BUS DISC, BOOTSTRAP, JLT, EXT. CLK., 2, COLEEN PROC. W.D., BUS DISC, BOOTSTRAP, JLT, EXT. CLK., 2, TRACE MEMORY

16K SYSTEM:

DYNABYTE RAM

| BANK SELECT | 1-8 | ope | en: | 9 | on |
|-------------|-----|-----|-----|-----|----|
| WRT PROT | 1-5 | ope | n | | |
| BANK 3&4 | Set | to | СX | å | FΧ |
| BANK 1&2 | Set | to | øø- | -11 | - |

32K SYSTEM:

| DYNABYTE | - | Set | as | above, except: |
|----------|---|-----|----|---------------------------|
| BANK 1&2 | | Set | to | FX & CX |
| BANK 3&4 | | Set | as | desired - See Address Map |

IMS RAM - 32K systems only

| J2 | | uWr | |
|----------|-----|-------|---------|
| Mem addr | | ø | (∅Ø-3F) |
| Jl | | on,sp | |
| J4 | | 8,4,2 | ,1 |
| J5 | | 2, sp | |
| Addr: | 7-6 | 3 | |
| | 5-4 | 3 | |
| | 3-2 | 3 | |
| | l-Ø | non | e |
| | | | |

DEVELOPMENT SYSTEM SWITCHES (continued)

DRC PROM CARD

D9-D16 n.c. D1-D8 diodes WAIT 1-14 jumpered Select 2-7,3-6 jumpered -----

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- 16K PROM CARD (Cromemco)
 - Bank Ø-7 off OUT off Al5 off DMA off Al4 on Disable ROM's Ø-7 Wait Disable

TUART optional

1,3-6,8,10 ON 2,7,9 OFF

BYTESAVER optional

Al5-Hi Al4-Lo Al3-Hi AØ-BF Wait N.C. Protect - Off when programming

TERMINAL FORMAT

The 685Ø serial communications ports are configured by software upon reset as follows:

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7 Data bits 1 Stop bit Even Parity

Baud rate is set by switches on the trace memory interface card. Recommended speed when used with TRACE MEMORY, 19,200 baud.

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INTERRUPT HANDLING

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If RAM resides at interrupt vector locations FFF8-FFFF, LNBUG will always point IRQ's and NMI's at it's own programs upon cool or cold reset. HIRQ (FFF8 and 9) is then used for the user IRQ vector. If ROM resides at FFF8-FFFF, LNBUG will give the user the option to have Colleen vectors point at LNBUG. If the option is selected, Colleen vector VIMIRQ (216) will point at LNBUG's IRQ routine and USIRQL (C288) will point at the user IRQ routine. Also, thereafter, anytime single step is selected, LNBUG will use NMI vectors at VVBLKI (222). If option is not selected, vectors for Colleen will be untouched and "ROMFLG" will be reset. "ROMFLG" controls options in setting single step vectors and in selection either HIRQ or USIRQ for IRQ vectors after going through the LNBUG IRQ routine.

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CAUTIONS:

If interrupts are to occur while LNBUG is running, no interrupt routine should use zero page locations $8\emptyset-9F$ as this will crash LNBUG.

June 3, 1980 Page Two

11. <u>Single Step</u> - With Colleen ROM O.S. you must use the new address PROM to prevent single stepping at E7XX.

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12. <u>Relocation Registers</u> - Seven more relocation registers have been added to allow flexible debugging of several relocatable program sections.

EX: Setup - 1000,2Y Run - 1000Y2/Q Y=0-7 -

- 13. Break Key now sends a break condition to the aux. port when in the "\$" mode.
- 14. Problems with proceeding from a breakpoint and using multiple passes through a breakpoint or single step have been fixed.
- 15. <u>Run Subroutine Command</u> To run a subroutine and return to LNBUG upon the RTS, specify as ADR G@ or G@.
- 16. Enable Interrupts during LNBUG. Set the Z command. To reset specify ZX.
- 17. User can initial stack at desired location by typing "S" and then MSD of stack address immediately following reset button. LNBUG then does a cold start. A cool or warm start reinitializes stack at previous value. This feature is useful for development of programs where no memory resides at 1FF.
- 18. PROM programming has been moved to RAM. BYTSVN must be downloaded first before command can be used.

OTHER DEVELOPMENT SYSTEM CHANGES AND ADDITIONS June 3, 1980

- 1. New baud rate switches to be mounted on front panels.
- 2. Colleen processor card with Colleen chips.
- 3. Colleen address map and RAM requirements have been changed.
- 4. Changes to gradually be implemented on the TMI cards add higher quality connectors, Aux. port polarity switch, separate connector to allow the use of a terminal for LNBUG only and one for the trace memory.
- 5. Trace memory See trace memory manual.
- 6. Updated trace memory manual and LNBUG 5 manual.

For answers to questions, please contact Larry Nicholson, Cyan Engineering, Grass Valley (916) 273-6194.

NEW FEATURES OF LNBUG 6.0 June 3, 1980

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LNBUG 6 is an updated version of all previous LNBUG monitors, obviously expected to be as complete as ever needed but undoubtedly due to change:

- <u>Cool Reset</u> Resets everything except patches, breakpoints, and macro commands. Type "C" upon reset.
- Macro Command Files Save up to eight command lines for later use without retyping addresses, data, etc. (J command)
- 3. Loading and Writing to tape now has a switch (") to allow selection of either terminal port or auxiliary port.
- 4. Uploading and Downloading and Other PDP11 Communications -LNBUG 6 contains a simple method to communicate with a timeshare system including uploading from LNBUG and downloading to LNBUG. For previous LNBUG 3 users, ∧ D replaces ∧ S for return to LNBUG.
- 5. <u>Read-Modify Sequence</u> When listing a line at a time using the "/" immediate command, the beginning of the last line is opened for modification rather than the address that the whole listing began.
- 6. Zero Page RAM To allow development of Stella (Video Computer System) programs, the required LNBUG zero page RAM has been moved from ØØ-Ø3 to 8Ø-96. (Stella has no RAM at the bottom of zero page). This should make little difference in user program operation as LNBUG retains a pseudo zero page for the user. See "CAUTIONS" for further details.
- Carriage Return Delay Instead of delaying a clock-dependent time for hard copy, the delay program simply outputs 10 null characters instead - (Baud rate dependent).
- 8. Interrupts and Single Stepping A correction has been made to allow single stepping through an interrupt program without fouling up the interrupt status. However, due to inherent conflictions of hardware and the variable complexity of interrupt structures versus a debug monitor (real time versus stop time), problems may still arise. It is recommended that a trace analyzer be used for real time operations.
- 9. <u>Colleen RAM O.S.</u> See section at end of manual for update on interrupt vector handling. Replace Address Map "ROM" with Colleen Address Map "PROM."
- 10. RAM Relocation RAM has been moved to CØØØ-C2FF.

NEW FEATURES OF LNBUG 6.0

December 12, 1979

LNBUG 6 is an updated version of all previous LNBUG monitors, obviously expected to be as complete as ever needed but undoubtedly due to change!

- <u>Cool Reset</u> Resets everything except patches, breakpoints, and macro commands. Type "C" upon reset.
- Macro Command Files Save up to eight command lines for later use without retyping addresses, data, etc. (J command)
- 3. Loading and Writing to tape now has a switch (") to allow selection of either terminal port or auxiliary port.
- 4. Uploading and Downloading and Other PDP11 Communications -LNBUG 6 contains a simple method to communicate with a timeshare system including uploading from LNBUG and downloading to LNBUG. For previous LNBUG 3 users, ^ D replaces ^ S for return to LNBUG.
- 5. <u>Read-Modify Sequence</u> When listing a line at a time using the "/" immediate command, the beginning of the last line is opened for modification rather than the address that the whole listing began.
- 6. Zero Page RAM To allow development of Stella (Video Computer System) programs, the required LNBUG zero page RAM has been moved from ØØ-Ø3 to 8Ø-FF. (Stella has no RAM at the bottom of zero page). This should make little difference in user program operation as LNBUG retains a pseudo zero page for the user. See "CAUTIONS" for further details.
- Carriage Return Delay Instead of delaying a clock-dependent time for hard copy, the delay program simply outputs 10 null characters instead - (Baud rate dependent).
- 8. Interrupts and Single Stepping A correction has been made to allow single stepping through an interrupt program without fouling up the interrupt status. However, due to inherent conflictions of hardware and the variable complexity of interrupt structures versus a debug monitor (real time versus stop time), problems may still arise. It is recommended that a trace analyzer be used for real time operations.
- 9. <u>Coleen ROM O.S.</u> See section at end of manual for update on interrupt vector handling. Replace Address Map "ROM" with Coleen Address Map "PROM."
- 10. RAM Relocation RAM has been moved to $C \emptyset \emptyset \emptyset$.
- 11. <u>Single Step</u> With Coleen ROM O.S. you must use the new address PROM to prevent single stepping at E7XX.

NEW FEATURES OF LNBUG 6.0 (continued) Page Two

- 12. PROM programming capability has been moved to system hard disk and out of PROM.
- 13. Addresses of stop and start addresses for calling list routines have changed to the following:

| Start ADL | |
|-----------|--|
| Start ADH | |
| Stop ADL | |
| Stop ADH | |
| | Start ADL Start ADH Stop ADL Stop ADH |

- 14. Half of zero page is now saved to allow proper stack operation with the VCS - LNBUG uses no more stack than an interrupt before zero page is saved.
- 15. Hitting the break key while in "PDP11" mode will send a break out aux. port.
 16. @ Suffix runs subroutines when added to "G" command. OTHER DEVELOPMENT SYSTEM CHANGES AND ADDITIONS
 - 1. New baud rate switches to be mounted on front panels.
 - 2. Coleen processor card with Coleen chips.
 - 3. Coleen address map and RAM requirements have been changed.
 - 4. Changes to gradually be implemented on the TMI cards add higher quality connectors, Aux. port polarity switch, separate connector to allow the use of a terminal for LNBUG only and one for the trace memory.
 - 5. Trace memory See trace memory manual.
 - 6. Updated trace memory manual and LNBUG 6 manual. (Please change pages supplied.)

For answers to questions, please contact Larry Nicholson, Cyan Engineering, Grass Valley (916) 273-6194.

NEW FEATURES OF LNBUG 5.0 August 23, 1979

LNBUG 5 is an updated version of all previous LNBUG monitors, obviously expected to be as complete as ever needed but undoubtedly due to change!

- <u>Cool Reset</u> Resets everything except patches, breakpoints, and macro commands. Type "C" upon reset.
- <u>Macro Command Files</u> Save up to eight command lines for later use without retyping addresses, data, etc. (J command)
- 3. Loading and Writing to tape now has a switch (") to allow selection of either terminal port or auxiliary port.
- 4. Uploading and Downloading and Other PDP11 Communications -LNBUG 5 contains a simple method to communicate with a timeshare system including uploading from LNBUG and downloading to LNBUG. For previous LNBUG 3 users, ∧ D replaces ∧ S for return to LNBUG.
- 5. <u>Read-Modify Sequence</u> When listing a line at a time using the "/" immediate command, the beginning of the last line is opened for modification rather than the address that the whole listing began.
- 6. Zero Page RAM To allow development of Stella (Video Computer System) programs, the required LNBUG zero page RAM has been moved from ØØ-Ø3 to FC-FF. (Stella has no RAM at the bottom of zero page). This should make little difference in user program operation as LNBUG retains a pseudo zero page for the user. See "CAUTIONS" for further details.
- Carriage Return Delay Instead of delaying a clock-dependent time for hard copy, the delay program simply outputs 10 null characters instead - (Baud rate dependent).
- 8. Interrupts and Single Stepping A correction has been made to allow single stepping through an interrupt program without fouling up the interrupt status. However, due to inherent conflictions of hardware and the variable complexity of interrupt structures versus a debug monitor (real time versus stop time), problems may still arise. It is recommended that a trace analyzer be used for real time operations.
- 9. Colleen ROM O.S. See section at end of manual for update on interrupt vector handling. Replace Address Map "ROM" with Coleen Address Map "PROM".
- 10. RAM Relocation RAM has been moved to $C\emptyset\emptyset\emptyset$ -C2FF.
- 11. <u>Single Step</u> With Colleen ROM O.S. you must use the new address PROM to prevent single stepping from D800-FFFF

OTHER DEVELOPMENT SYSTEM CHANGES AND ADDITIONS August 23, 1979

- 1. New baud rate switches to be mounted on front panels.
- 2. Colleen processor card with Colleen chips.
- 3. Colleen address map and RAM requirements have been changed.
- 4. Changes to gradually be implemented on the TMI cards add higher quality connectors, Aux. port polarity switch, separate connector to allow the use of a terminal for LNBUG only and one for the trace memory.
- 5. Trace memory See trace memory manual.

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6. Updated trace memory manual and LNBUG 5 manual

For answers to questions, please contact Larry Nicholson, Cyan Engineering, Grass Valley (916) 273-6194.