The RAINBOW Gold Chip Specifications

George Wang

Atari Semiconductor Group

October 28, 1983

TABLE OF CONTENTS

TABLE OF CONTENTS (con't)

TABLE OF ILLUSTRATIONS

TABLE OF ILLUSTRATIONS(con't) Page Number

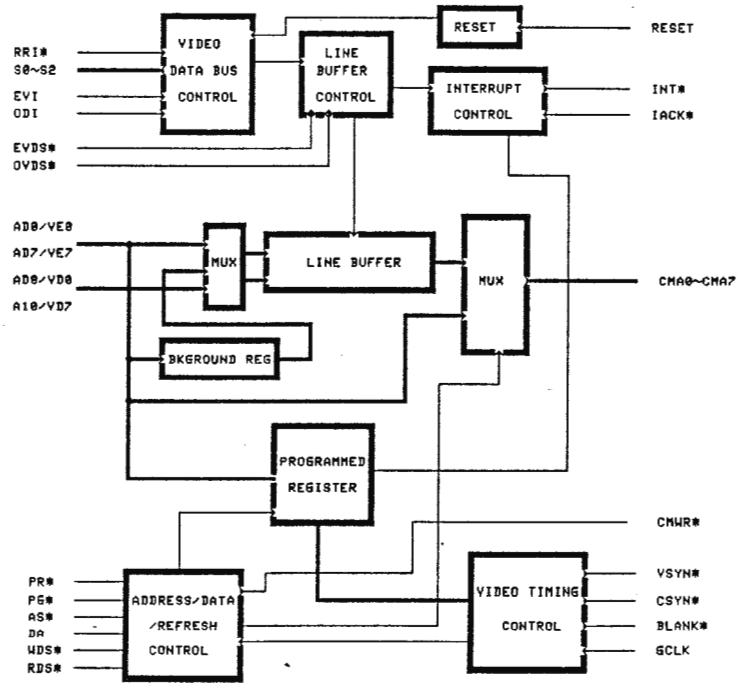
1. GENERAL DESCRIPTION

The Rainbow-Gold chip contains counters, finite state machines and a long line buffer which creats standard video timing signals to control the CRT, and graphics data to address the Color Map chip. The Color Map chip will provide display information to the CRT. To perform the graphics display capability it requires that the Rainbow-Gold chip works with the Rainbow-Silver chip.

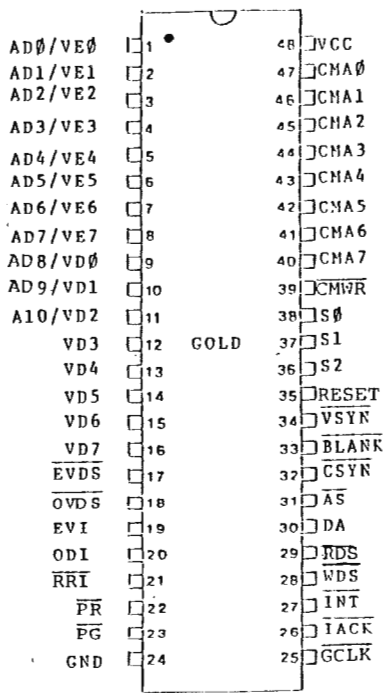
2. FEATURES

@ High resolution display (typical 640 x 480 pixels).
@ 256 displayable color from a total of 4096 in Color Map chip.
@ Dynamic memory refresh control.
@ On-chip line buffer relax timing constraints.
@ Programmable vectored interrupt and line interrupt.
@ Programmable Horizontal display (512 to 768 pixels).
@ Programmable Vertical display (384 to 638 lines).
@ Programmable background register.
@ RGB or NTSC/PAL video interface capability.

3. BLOCK DIAGRAM



4. PIN ASSIGNMENT



5. PIN DESCRIPTION

Pin Name	Type	Pin#	Function
AD0/VE0 ~ AD7/VE7	I/O	1-8	These lines constitute the time multiplexed Address bus A0 to A7, Data bus D0 to D7 and Video Even pixel bus VE0 to VE7. The Address bus and Data bus are valid inputs when the Processor Grant pin PG is LOW. While the status pins S0 to S2 indicate Refresh condition being active, the Address bus will be used as outputs to refresh the memory. The Interrupt vectors are put on Data bus when the Interrupt Acknowledge pin is aserted to LOW. Pixel data only are presented on the Video Even Pixel bus lines when the status pins S0 to S2 indicates video pixel condition being active.
D8/VD0 ~ A10/VD2	I/O	9-11	These lines constitute the time multiplexed Address bus A8 to A10, Data bus D8 to D9 and Video Odd Pixel bus VD0 to VD3. The function and validility of the Address bus and Data bus are described in the above section. The function of the Video Odd Pixel bus is described in the next section.
VD3-VD7	I	12-16	Combinations of VD0 to VD7 pins are used as the Video Odd Pixel inputs. Video data only are presented on these bus lines when the Status pins S0 to S2 indicate Video Pixel condition being active.
$\overline{\text{RRI}}$	I	17	Video bus Release(includes both video odd and even pixels bus); the falling edge of this input indicates that none of Silver chips use the Video bus to access the memory and valid video data from Silver chips are available on the video bus to be strobed.

PIN DESCRIPTION (con't)

Pin Name	Type	Pin#	Function
$\overline{\text{EVDS}}$	I/O	18	Even pixel Video Data Strobe; it strobes even pixel data from the video bus into the line buffer. This pin is a bi-directional and active LOW signal. Only when the Even pixel Priority In input EVI is High in the Gold chip, then this pin will be an output. Otherwise, it stays as an input.
$\overline{\text{OVDS}}$	I/O	19	Odd pixel Video Data Strobe; it strobes odd pixel data from the video bus into the line buffer. This pin is a bi-directional and active LOW signal. Only when the Odd pixel Priority In input EVI is High in the Gold chip, then this pin will be an output. Otherwise, it stays as an input.
EVI	I	20	Even pixel priority in; when this input is HIGH, it means the Gold chip gets priority and has to move data from the Background register to the even pixel position in the line buffer.
ODI	I	21	Odd pixel priority in; when this input is HIGH, it means the Gold chip gets priority and has to move data from the Background register to the odd pixel position in the line buffer.
$\overline{\text{PR}}$	I	22	Processor Request; when this input input is LOW, it indicates the CPU wants to access the programmable registers in the Gold chip or write color information to the Color map chip through the Gold chip.

Pin Description (con't)

Pin name	Type	Pin#	Function
$\overline{PG}$	I	23	Processor Grant; when the processor Request PR is LOW and the Gold chip is not using the video bus, then the Gold chip can set this output LOW to grant this bus to the CPU.
GND	I	24	Ground.
GCLK	I	25	Gold Chip Clock; the clock provides the basic timing for the Gold chip.
$\overline{IACK}$	I	26	Interrupt Acknowledge; it is used as a read strobe to strobe the interrupt vector onto the Data bus. It is an active LOW signal.
$\overline{INT}$	O	27	It is used to interrupt CPU when any not-masked interrupt condition occured in the Gold chip. This is an active LOW signal.
$\overline{WDS}$	I	28	Write Data Strobe; when it is LOW, it strobes data from the System bus into the Gold chip.
$\overline{RDS}$	I	29	Read Data Strobe; when it is LOW, CPU reads data from the System bus into itself.
DA	I/O	30	Data Acknowledge; it is used as an output to inform CPU that data transfer is completed. It is used as an input to indicate that a refresh cycle is finished.

Pin Description (con't)

Pin Name	Type	Pin#	Function
$\overline{AS}$	I/O	31	Address Strobe; This signal is used as an input to indicate that there is a valid address on the Address bus. When the Gold chip performs memory refresh cycle, it is used as an output to strobe the valid address on the system bus.
$\overline{CSYN}$	O	32	Composite Sync; this signal provides a composite sync waveform with the regular horizontal sync, equalization pulses and vertical serations in both interlaced and noninterlaced formats. This output is typically connected to the Horizontal input of a CRT.
$\overline{BLANK}$	O	33	This is an active LOW signal. It remains active for entire retrace interval. It is used to blank the video to a CRT.
$\overline{VSYN}$	O	34	Vertical Sync; this signal when active LOW, will initiate a vertical retrace. This output is connected to the Vertical sync input of a CRT.
RESET	I	35	Reset is an active HIGH signal which is used to either reset all Gold and Silver chips or indicate a bad address memory access by the Silver chip. When the interval of this active HIGH input is less than three clocks cycle, it will not be recognized as a valid input by Gold chip. When this HIGH interval lasts for three to ten clocks, it indicates a bad memory access. While this high is longer than 10 clocks cycle, it means to reset all Gold and Silver chips.

Pin Description (con't)

Pin Name	Type	Pin#	Function
S2-S0	O	36-38	These status lines provide information to the silver chip as follows:

S2	S1	S0	Description
0	0	0	Refresh Active
0	0	1	No operation
0	1	0	Abort memory cycle
0	1	1	Reset
1	0	0	Top of screen in Even field
1	0	1	Top of screen in ODD field
1	1	0	Pixel Active
1	1	1	Link Load Active

$\overline{\text{CMWR}}$	O	39	Color Map Write; when CPU accesses the Color Map chip, the address inputs A10 to A9 will be decoded in the Gold chip to enable the route from WDS input to CMWR output. This signal will strobe color data into the Color Map chip.
CMA7-CMA0	O	40-47	Color Map Address; when CPU accesses the Color Map chip, the address inputs A10 to A9 will be decoded to enable the route from address lines A8 to A1 to the color map address CMA7 to CMA0. Otherwise, These address lines are used for the regular video from the line buffer to address the color map.
VCC	I	48	VCC is the +5V power supply.

6. FUNCTIONAL DESCRIPTIONS

6.1 Overview

The Rainbow video graphics system is object based. All display activity is described in movable, variable-size, multimode objects. An object is like a sprite, but more general; like a combination of Antic's playfield and players. Objects are not limited in size, and can be reused in vertical sequence. Thus the display horizontal complexity is limited to the number of hardware objects supplied in the Silver chip (12 object processors are contained in each chip now), but is not limited vertically.

The screen is organized as an array of square pixels. The standard resolution for NTSC display is 640 horizontal by 480 vertical. All graphics and text fonts are represented in term of pixels of this size. The reduced space-resolution modes may turn out to be far more often used, but this fine grained description is chosen as a standard that should cover all our "standard-video" needs, on NTSC, PAL and RGB monitors, for some time.

The video system can produce up to 256 different colors from a total palette of 4096(16 levels of gray).

The Rainbow chip set performs the function of translating from digital representations of graphics into the time-sequenced signals necesary to address a Color Map chip which is drived a raster-scanned CRT. The Color Map chip will produce interlaced RGB digital video outputs. Three four bit D/A converters are needed to interface the Color Map to RGB monitors. Rainbow can be used with RGB to NTSC/PAL conversion devices, e.g. National LM1886 & LM1889 chip set, to produce composite video signals.

The video system communicates with memory over an asynchronous 16 bit bus as bus master. For dynamic memory refresh requirements, Rainbow will assert refresh request and a row address counter.

Each object processor in the Silver chip contains a parameter block and a pointer to video memory of the object representation. The video system can cause interrupts to main CPU to indicate error condition such as "Line Incompleted" and the NON-error condition "Programmed Line".

6.2 General Block Description

The Gold chip contains several functional blocks such as video timing, address/data/refresh control, video bus control, interrupt control, programmable registers, line buffer control and two line buffers. Basically, these blocks provides video timings, refresh address, interrupt information, status information, read/write control lines and color map addresses.

The video timing block provides software-adjustable signals such as composite Sync and Vertical Sync to drive different standards TV system (NTSC or PAL) or different resolution monitors. The Composite Sync signal waveform is composed of the regular horizontal sync, equalization pulses and vertical serrations in both interlaced and non-interlaced formats. This Composite Sync is connected to the Horizontal Sync input of a CRT. The Vertical Sync is connected to the Vertical Sync input of a CRT to initiate a vertical retrace. If the CRT only has one Sync input, then the Composite Sync is used to connect to this input. The Blank signal is also provided by this block to blank the video during either horizontal retrace or vertical retrace interval.

The Video data control block takes care of Even and Odd priority In chaining and provides Even video data strobe and Odd video data strobe signals to strobe video data from silver chips. Also this block provides status information such as reset, pixel active, refresh active, link load active top of screen in each field to the Silver chip through the S0, S1 and S2 lines.

The address/data/refresh control block provides the refresh address and refresh request (through Address Strobe AS pin) during Refresh Active condition. The Refresh Active condition is a status provided by Gold chip and indicated on the status lines S0 to S2. See details in the section 6.6 . When CPU requests to access a programmable register or the Color Map, the control block takes care of processor grant, time-multiplexed address and data, and read/write controls. If CPU wants to write data to the Color Map, this block will provide Color Map Write signal to the Color Map.

The Programmable register block contains 12 programmable registers which can be readable, writeable or read/writeable. Information like Background color, Interrupt mask, Interrupt vector, programmable line interrupt, Horizontal line size, Horizontal active video extension, Vertical front and back porch and Vertical active line extension are all included in this block.

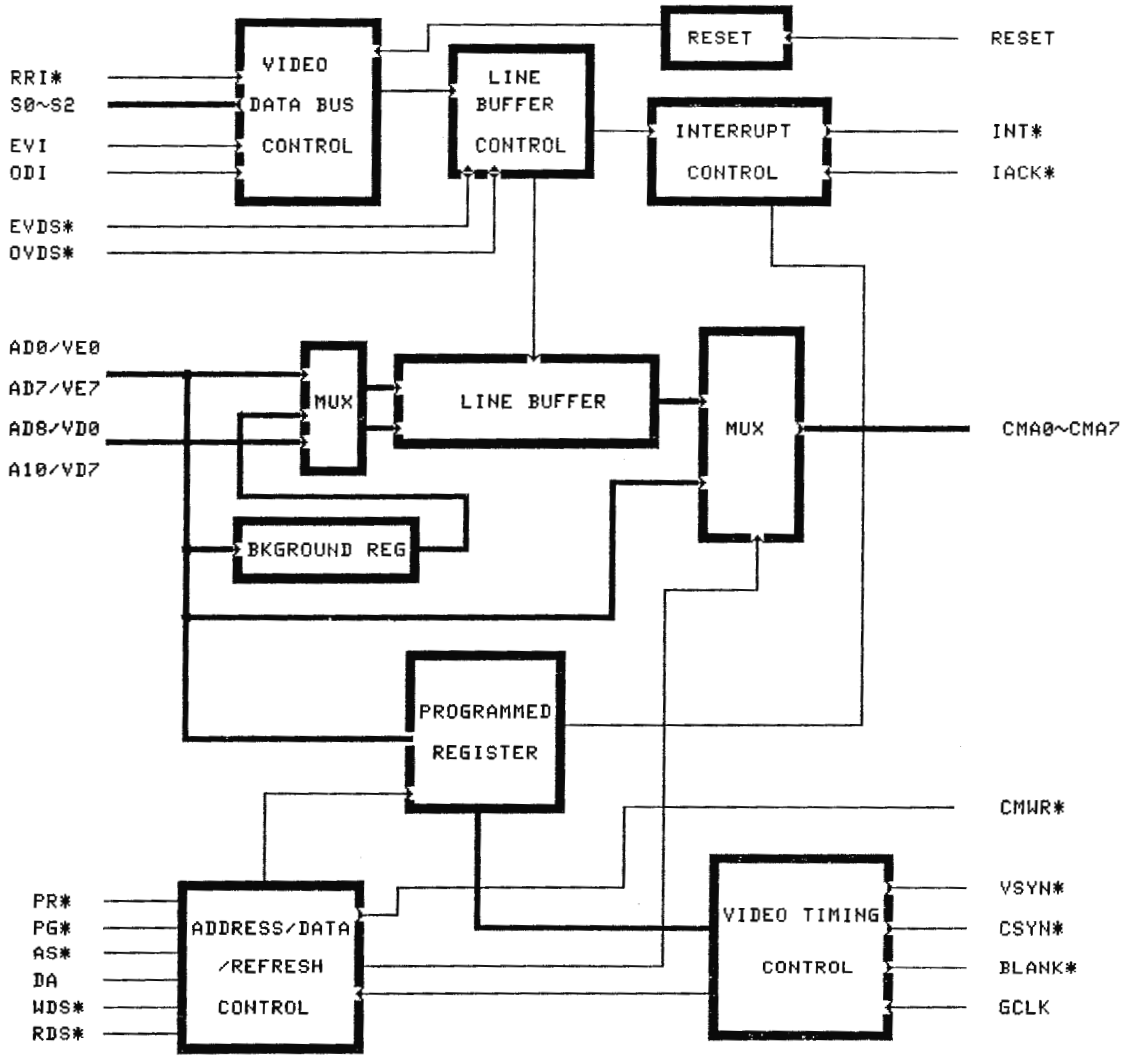
The Interrupt control block provides error-condition type interrupt such as line buffer incompletly filled and nonerror condition type such as programmed line interrupt. These interrupts can be masked by setting the corresponding bit in the Interrupt Mask register.

The Line Buffer block contains a long programmable line buffer with 16 bits in width and 581 bits in length. Since each pixel is represented by a 8 bits data, therefore this line buffer can contain up to 581 words (i.e. 1162 pixels). Each horiziontal scan line is allowed to program to display 768 pixels maximum. So this line buffer contains at least one and half horizontal line. There two pointers work with this line buffer. The Read pointer points to where to read data out of the buffer and the Write pointer points where to write data into the buffer. You may think this line buffer is a cyclic buffer conceptually.

The Line buffer control block cotains pointers control to move pointer along the Line buffer. It also detect the incomplete buffer filling and set the buffer incomplete interrupt bit in the Interrupt vector register.

Figure 1 shows the principal functional block in the Cold chip.

Figure 1. The Principal Functinal Block Diagram



6.3 Video Timings

6.3.1 CRT Basics

The principal function of the Video Timings, as described above, is to generate Horizontal and Vertical Syncs to drive a raster scan CRT. The name, so called raster scan CRT, is based on the fact that the image displayed on the CRT is biult up by generating a series of lines(raster) across the screen of the CRT. Usually, the electron beam starts to display from the upper left hand corner of the screen and simultaneously moves left to right and top to bottom to put a series of zig-zag lines on the screen.

When the beam reaches the end of a line, it is brought back to the beginning of the next line at a rate that is much faster than was used to generate the display line. This action is referred to as "Horizontal retrace". During this retrace period the electron beam is blanked (shut off) so that it does not appear on the screen.

While the beam is moving across the screen horizontally, it is also moving downward. Because of this, each successive line starts slightly below the previous line. When the beam finally reaches the bottom right hand corner of the screen, it retraces back to the top left hand corner. This retrace is referred to "Vertical retrace". During the vertical retrace period, the beam will be blanked too.

The horizontal and vertical movement of the electron beam is shown in the Figure 2.

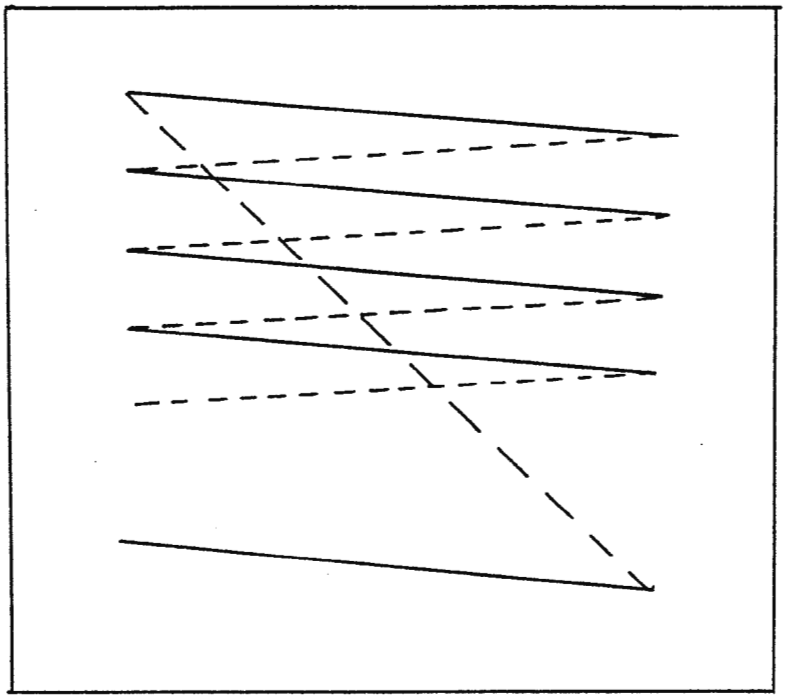
In an ordinary CRT, the time it takes for the beam to move from the top of the screen to the bottom and back again to the top is usually referred to as a "frame". In the United States, commercial televisions broadcast adopt NTSC system and use 15750 Hz as the horzitonal sweep frequency (63.5 microseconds per horizontal line) and 60 Hz as the vertical sweep frequency (16.67 milli-seconds per vertical frame).

Although the 60 Hz vertical frame and the 15750 Hz horizontal line are the standards used by the commerical broadcasts, they are by no means the only freqency at which CRT's can operate. As the matter of fact, many CRT operate around 18 KHz to 22 KHz horizontal frequency. As the horizontal frequency increases, the number of of horizintal lines displayed per fram increases. Hence, the resolution on the vertical axis increases. However, to display the high density grahics in a frame time, it needs an expensive high resolution CRT

Another alternative to display the high resolution graphics is using the "interlacing" method. The United States commerical TV stations adopts this method to broadcast their TVs. By dividing the 63.5 microsecond horizontal line rate into the 16.67 millisecond vertical frame rate, it will be 252.5 line in a vertical frame. At first, the half line may seem a bit odd, but actually it allows the resolution on the CRT to be effective doubled. This is done by inserting a second set of horizontal lines between the first set (called interlacing). Each set of horizontal lines is called "field". In the commerical TV system, first all of the even-numbered lines are displayed: 0, 2, 4,....524. This set is called Even field. Then all the odd-numbered lines: 1, 3, 5,...525. This set is called Odd field. Figure 3 shows the inter-lacing method.

Although interlacing provides higher resolution, it also has some disadvantages. First of all, the circuits required to generate the extra half horizontal line per frame is quite complex when compared to a noninterlaced design. Next, the overall vertical refresh rate is half that of a noninterlaced display. As a result, flicker may result when the CRT uses high speed phosphors. Therefore, whether to use a interlacing method, the phosphor's persistance on the CRT screen is an important factor.

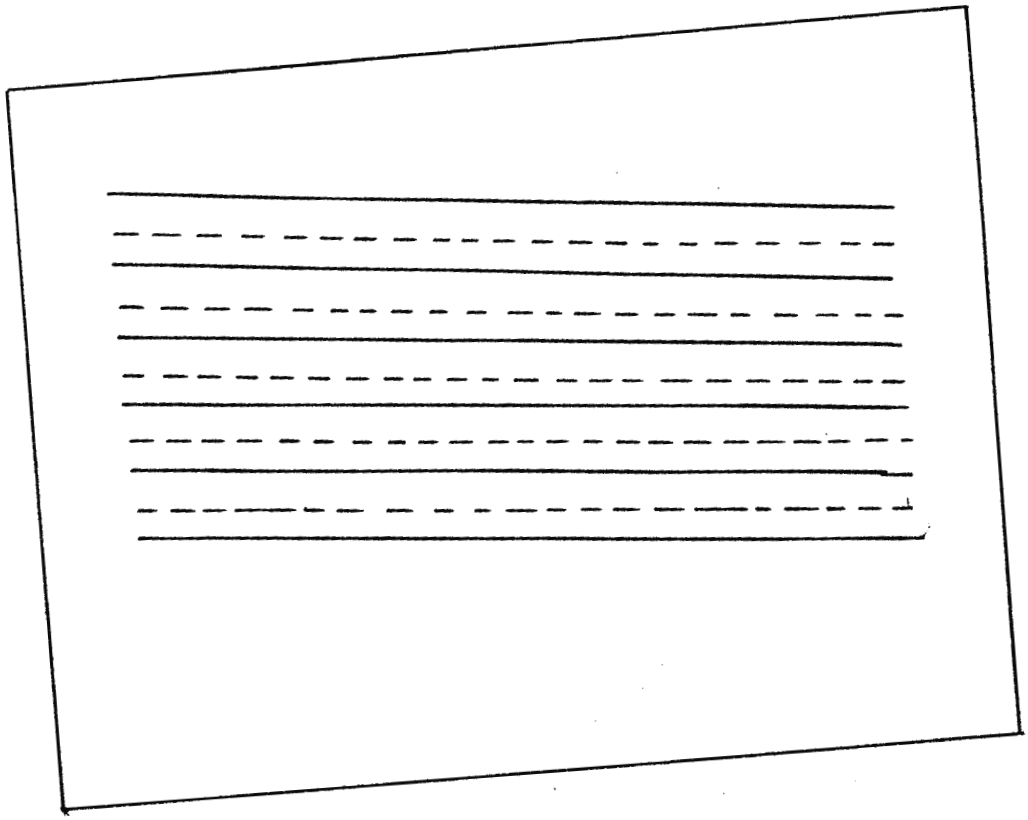
Figure 2. Raster scanning scheme



DISPLAYED LINES

RETRACE LINES

Figure 3. Interlacing method



EVEN FIELD

ODD FIELD

(retrace lines not shown)

6.3.2 Screen format

The first thing the Gold chip must do is to generate pulses that define the horizontal line timing and the vertical frame timing. This is usually done by defining a horizontal line in terms of the pixel dot clock and a vertical line in terms of the horizontal scaning line.

In general, a horizontal line can be divided into the visible video part and the blanking part. Further more, the visible part is divided into the active video and active video extension. The blanking part is divided into the horizontal front porch, horizontal sync, the horizontal back porch and horizontal back porch extension. The timing details will be explained in the "Horizontal timing" section.

A vertical line can be divided into the visible part and the blanking part, too. The visible part is composed of the active video line and the active video line extension. The blanking part is composed of the vertical front porch, the vertical sync, the equalizing pulse interval and the vertical back porch. The timing details of this vertical frame will be explained in the "Vertical timing" section.

The screen format is shown in the Figure 4.

6.3.3 Horizontal timing

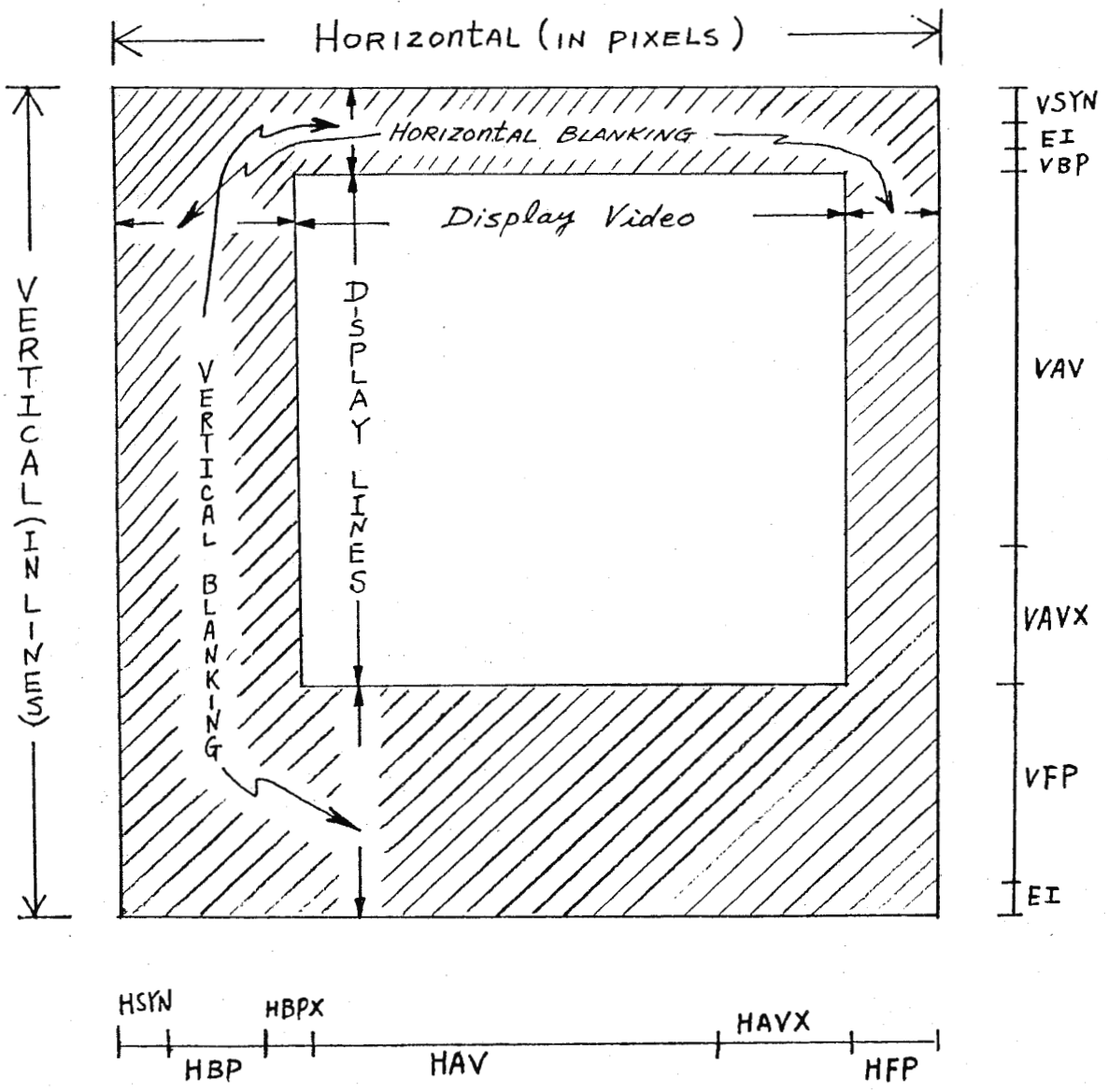
The timing of a horizontal scanning line is measured by the video pixel clock. The part of horizontally displayable and blanking area is programmable in term of the pixel clock.

Figure 5 shows the wavefrom and timings of the horizontal scaning line.

The Active Video part is the period that the video data is displayed on the CRT screen actively. The duration of this active video part is 512 video pixels long.

The Active Video extention part is used for extending the active video period. The duration of this period is programmable. It can be programmed from zero to 256 video pixels long. Therefore, the total horizontally displayable dimension of the screen may be from 512 pixels to 768 pixels wide.

Figure 4. Screen format of CRT.



** Here notations HAVX, HLS, HBPX, VAVX, VFP and VBP for programmable registers indicate which part of picture they control.

The Horizontal Front Porch is the number of video pixel delays before the Horizontal Sync. So, sometimes, it is called Horizontal Sync Delay. The times of this period is not programmable but depends on the total video scan lines on the screen which will decide the total pixel clocks in a horizontal scanning line. In other words, the duration of this period is equal to the total pixel clocks minus the sum of pixel clocks of the active video and Horizontal Sync and Horizontal back porch.

The Horizontal Back Porch is the number of video pixel delays after the Horizontal Sync. This interval is also called Horizontal Scan Delay. This interval consists of regular back porch and back porch extension. The duration of regular back porch is 32 video pixel long and the back porch extension can be programmed from none to 32 pixel long.

The Horizontal Sync is used for initiating the electron beam retrace from the right hand side back to the left hand side of the screen. The duration and frequency of this interval varies during a frame time.

During the Vertical display, Vertical front porch and Vertical back porch period, the duration of this Horizontal Sync interval is 52 pixels long.

During the Equalizing Pulse Interval, the duration of the Horizontal Sync is only the half of the regular Horizontal Sync. However, the frequency is doubled. In other words, the Sync pulse only has 26 pixel clock wide, but Sync occurs twice during a regular horizontal scanning time(63.5 microseconds).

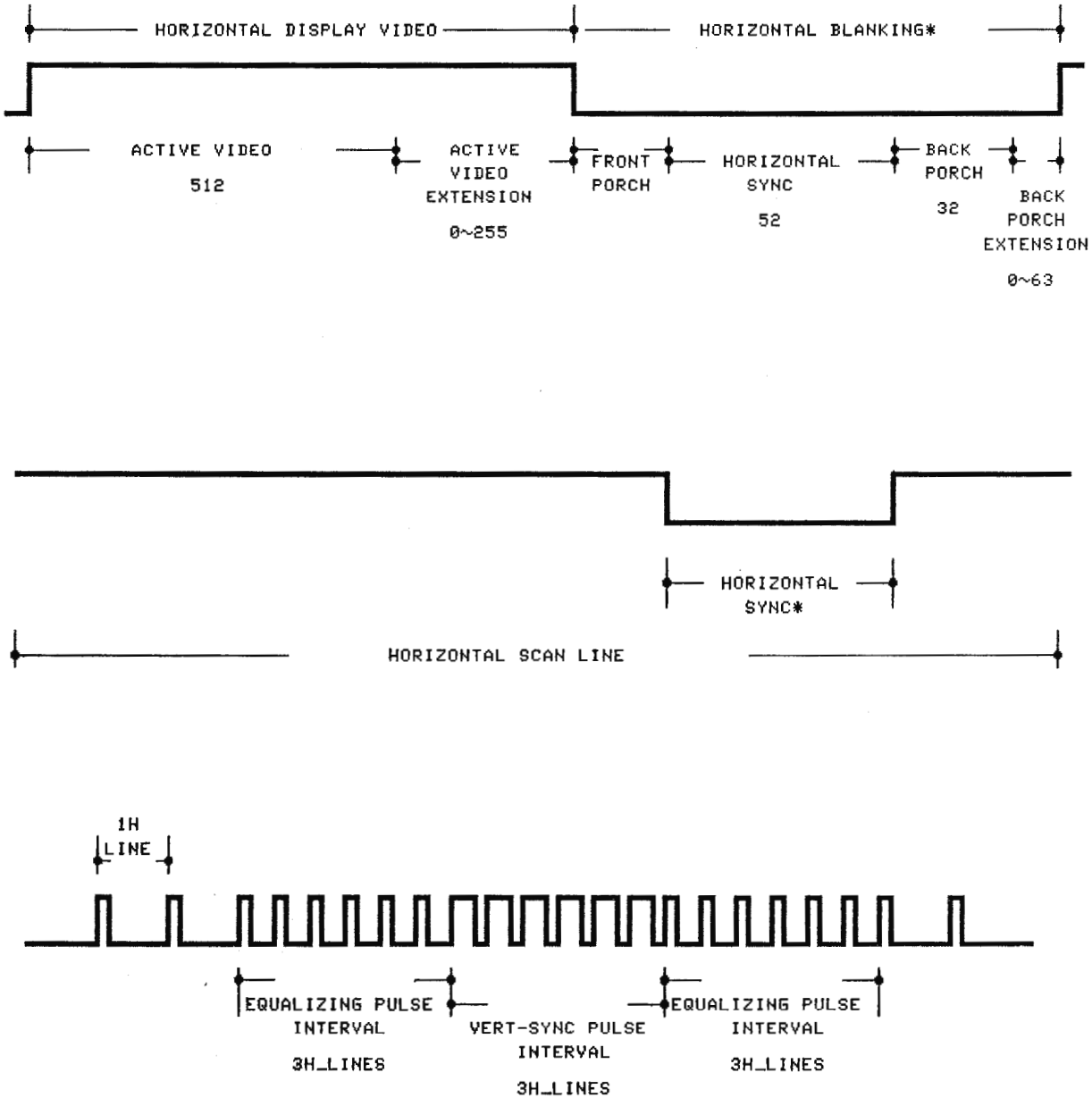
During the Vertical Sync period, the duration of this Horizontal Sync is 47% of a horizontal time and the frequency is doubled. So the Sync is 27.31 microseconds long and occurs twice a horizontal line time.

The combination of these regular horizontal Sync, equalizing-pulse and vertical serrated horizontal Sync is called the Composite Sync.

The total number of video pixel clocks in a horizontal scan line depends on how many scan lines in a frame which includes both odd and even fields. The total scan line can be programmed in the Horzontal Line Size register. This number is from 512 to 725 lines.

The block diagram in the Figure 6 shows the logic circuit generation of the Composite Sync and Horizontal Blank.

Figure 5. The Waveform and Timings of the Horizontal Scanning line.



6.3.4 Vertical timing

The timing of a Vertical frame is measured by the horizontal scan line. The part of vertically displayable and blanking period is programmable in terms of sacn line.

The waveform and timings of the vertical frame is shown in the Figure 7.

The Active Video line part is the period that video data is displayed actively in a vertical frame. The duration of this active video line part is 240 scan lines long.

Obviously, the active video line extention part is used for extending the active line period. The duration of this interval can be programmed from none to 64 horizontal scan lines. So the total vertical displayable dimension of the screen may be from 240 lines to 284 lines long.

The Vertical Front Porch is the number of sacn line delays before the Vertical Sync. It is also called the Vertical Sync Delay. The duration of this interval can be programmed from none to 32 scan lines long.

The Equalizing-pulse interval is used for generating serrated horizontal Syncs during this interval. These serrated Syncs are used to achieve uniform firing of the CRT vertical retrace. This interval is 3 regular horizontal scan lines long. Also this interval immediately precede and follow the vertical Sync.

The Vertical Back Porch is the number of scan lines delays between the Vertical Sync and the displayed information. This interval is called Vertical Scan Delay, too. This interval can be programmed from none to 32 scan lines. In the Odd scan line field, one more line is added to the programmable valus. In other words, the Vertical Back Porch will be at least 1 to 32 scan lines long at most.

The Vertical Sync is used to trigger the vertical sweep generator at te CRT, initating the return of the the beam from the bottom to the top of the screen at the end of each field. The duration of this interval is 3 horizontal scan lines long.

When the interlacing method is used for display on the CRT, it needs to creat the Vertical Sync for each field at different timings. The timing difference between falling edge of two Syncs is half scan line timing.

The block diagram of the logic circuit of generation of Vertical Sync and Vertical blank is given in the Figure 8.

6.3.5 interlacing/noninterlacing mode

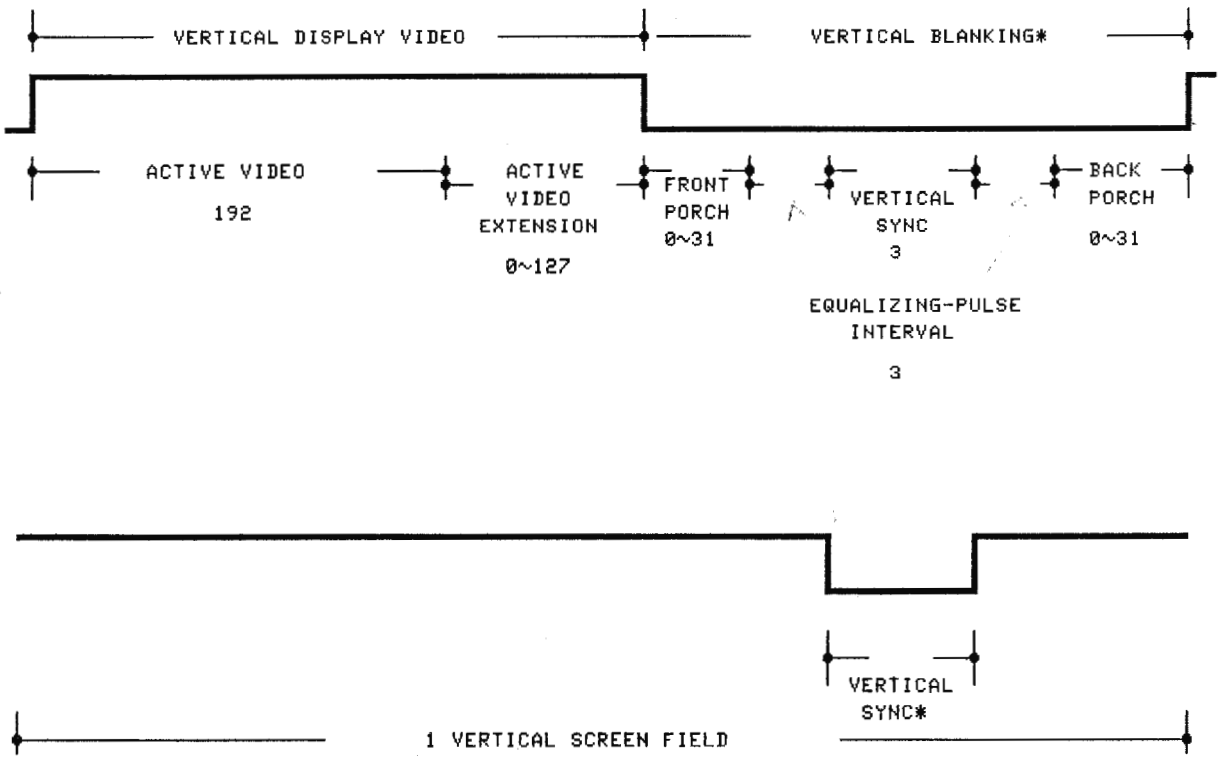
Rainbow Gold will generate interlaced video signals for full vertical resolution on normal (NTSC and monitor) displays. There is provision for use in non-interlaced system. If the non-interlaced bit is set, Rainbow generates even fields only.

In other words, every field is identical (rather than alternating between even and odd). Data on the screen is what would have been generated for the even field in the interlace mode. Gold chip will generate status information indicating even field only.

The Silver chip must be programmed to repeat its horizontal scan line twice in a frame. The value in the horiztal line repeat register is 1.

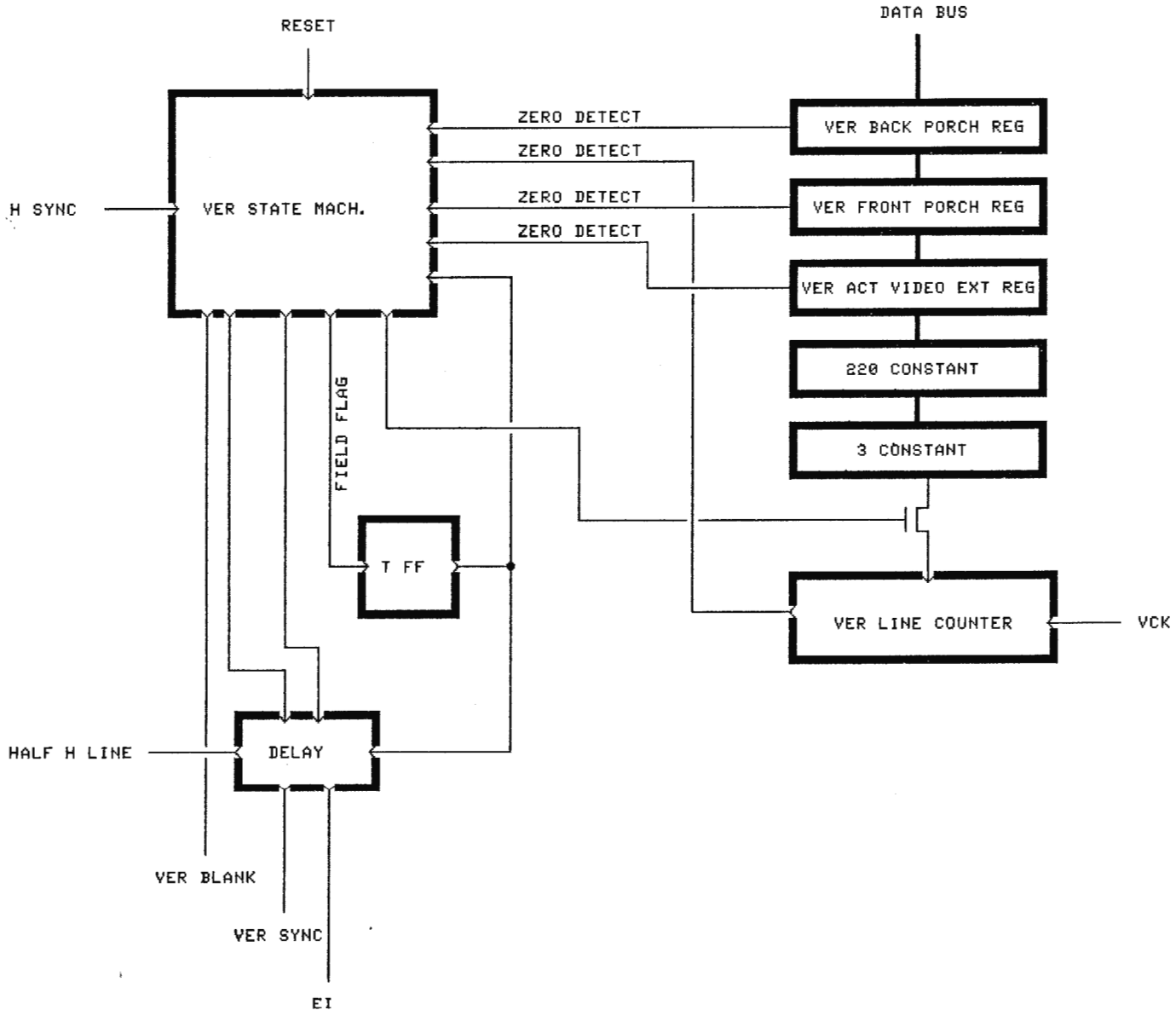
Rainbow will operate initially and by default in interlace mode (i.e. until non-interlace is explicitly set).

Figure 7. The Waveform and Timings of the Vertical Frame.



** THE NUMBERS SHOWN IN THIS FIGURE IS FOR EACH FIELD AND NUMBERS IN PROGRAMMED REGISTER IS FOR A FRAME.

Figure 8. Block diagram of generation of Vertical Sync and Blank.



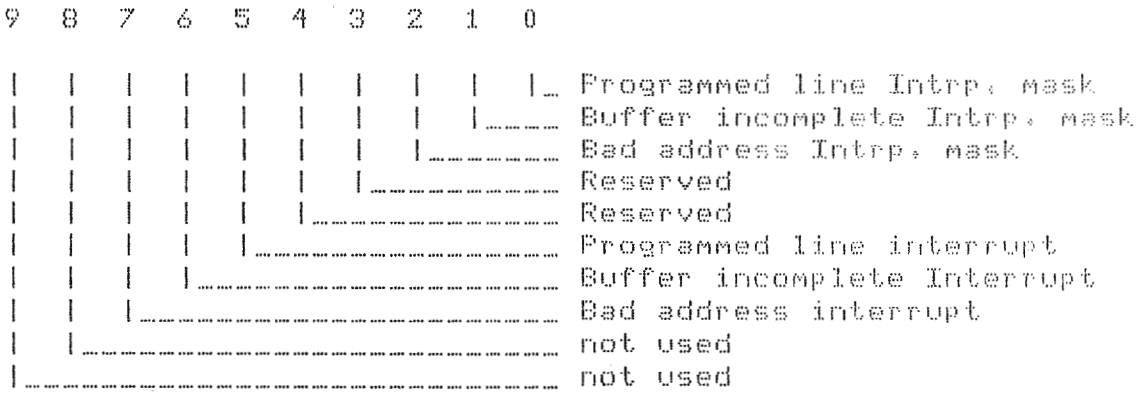
6.4 Interrupt Control

Rainbow Gold generates interrupts for programmed line, line buffer incomplete and bad memory address (no data acknowledge back from a memory fetch cycle). A program can get an interrupt each field by setting the programmed line interrupt for the last line of the field.

6.4.1 Interrupt Status and Interrupt mask

Rainbow Gold chip contains an Interrupt Status and Mask register. The Interrupt Mask is used for masking the occuring interrupt. By setting a bit in the Interrupt Mask position (the first three least significant bits in the Interrupt Status/Mask register), the corresponding interrupt condition will not occur in the interrupt pin.

The Interrupt status is used for storing the interrupt condition if it is not masked by the user. There are three interrupt conditions: programmed line, line buffer incomplete and bad memory address. Bit location of these interrupt conditions in the Interrupt Status/Mask register is listed as follows.



Whenever the Gold chip internally detects a line buffer is incompletely filled, it will set bit 5 in the Interrupt Status/mask register if bit 1 is not set. Also the current line counter always compares its content with the Programmed Line Interrupt register. If they match and bit 0 is not set, bit 5 will be set in the Interrupt Status/Mask register. If Bad memory address control block detects a bad address and the bit 2 is not set, then bit 7 will be set.

6.4.2 Interrupt vector

Most high performance CPUs contain the mechanism to accept an eight bit vector during interrupt acknowledgement. This vector will direct the CPU to the appropriate interrupt service routine. The interrupt vector presented to the CPU is created by logically "OR gating" the Interupt vector register with a value representing the type of interrupt. Rainbow will generate different vector depending on the value in the Interrupt vector register. Bit zero of the interrupt vector will always be set to zero.

The interrupt type value that is "ORed" with the vector register is:

Programmed Line Interrupt:	0
Buffer Incomplete Interrupt:	2
Bad Address Interrupt:	4

Once any interrupt bit (bit 5 to bit 7) is set in the Interrupt Status/Mask register, an active Low interrupt signal INT is generated to CPU. The CPU will send an active LOW interrupt acknowledge signal IACK back. When the Gold chip receives the IACK, it will load the interrupt vector onto the data bus lines. Then CPU will send a Read Data Strobe signal RDS to read this byte interrupt information. Then the Gold chip can send a Data Acknowledge signal DA to trigger CPU to finish the read cycle and interrupt cycle.

After the interrupt vector is loaded on the Data bus and CPU's Read Data Strobe goes HIGH, the interrupt status bits in the Interrupt Status/mask register will be reset.

Figure 9 will show the timing diagram of the interrupt sequence.

The main CPU can be interrupted on an arbitrary line number which helps synchronize the CPU with horizontal video rate. The CPU will be interrupted every field at a specific line number zero begins at the top of screen and the last displayed line is 479. The programmable Line Interrupt register is a ten bits register.

Because of interlace, the Programmable line interrupt will occur on the specified line in the even (odd) field, line is even- (odd-) numbered, and on the the next line (line number one greater) in the odd (even) field. For instance, if the number is 120 in the register, the CPU will be interrupted at line 120 in the even field and line 121 in the odd field.

The Programmed line interrupt will occur at the beginning of that specific line.

The Programmed line interrupt can be used as a "field interrupt" by setting it for line 480(for NTSC system; different number for other TV system such as PAL system). This will interrupt on the last line of every field.

The Programmed line interrupt may also be set for a line number greater than the last visible line, and will then occur within the vertical blanking interval. Any line number up to the total number of lines in a frame, visible or blanked, may be used. The maximum line number is programmable in the Horizontal Line Size register.

The block diagram is shown in the Figure 10.

Figure 9. Timing diagram of Interrupt control.

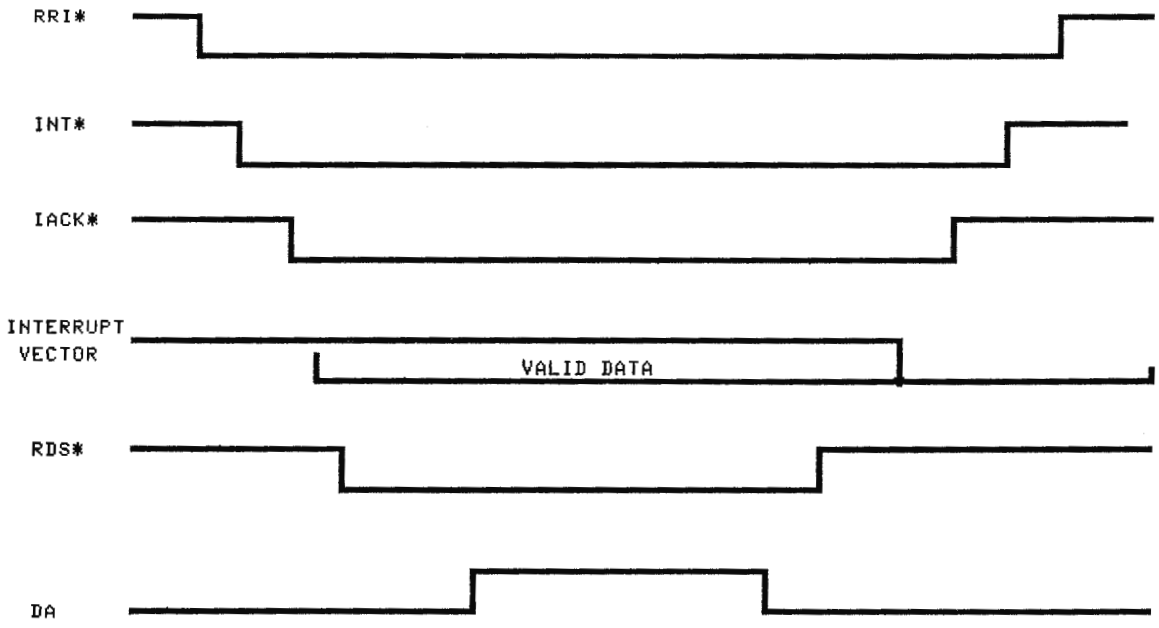
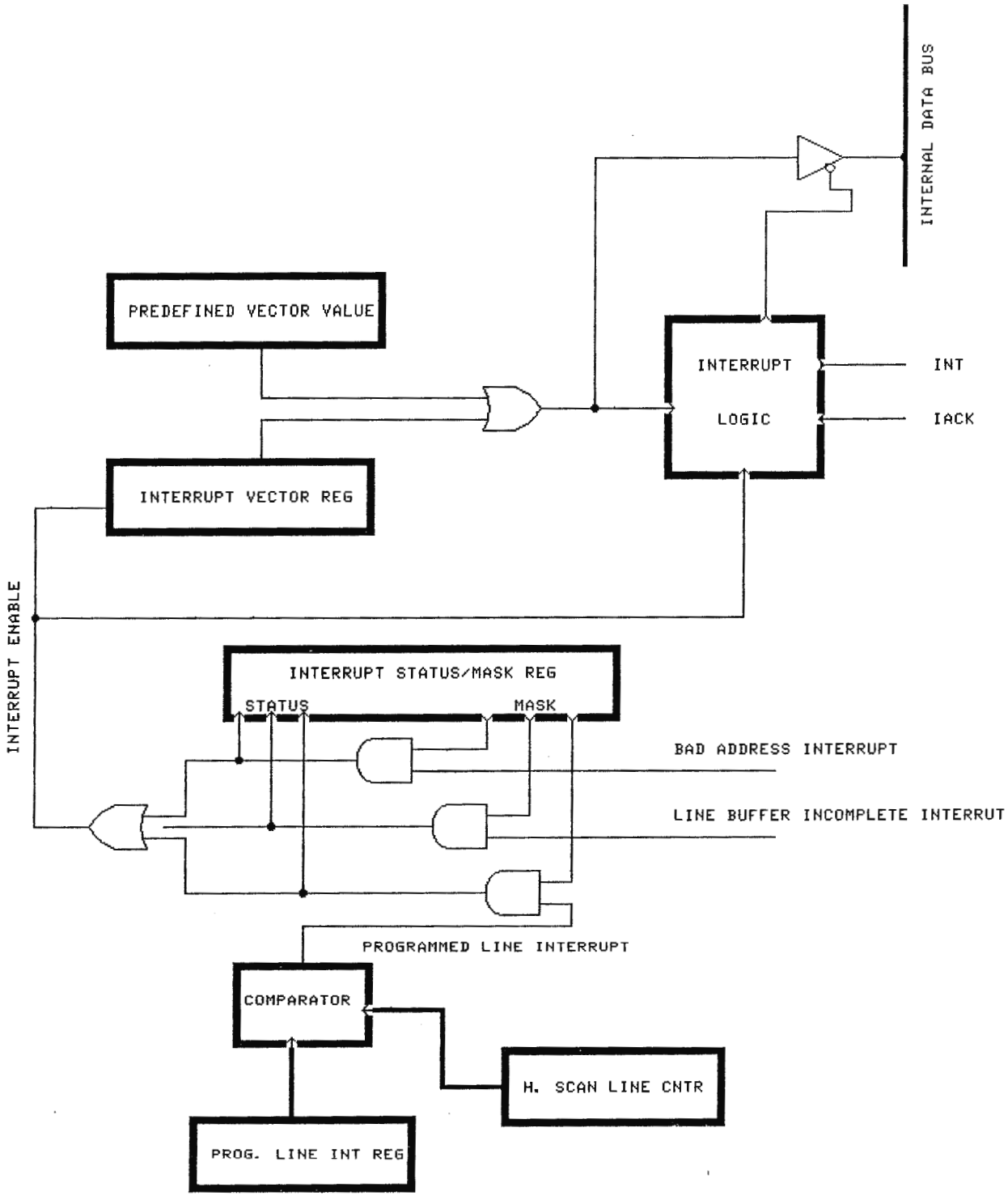


Figure 10. Block diagram of Interrupt Control logic circuit.



6.5 Video Data Control

The principal function of this video data control is control the video bus interface signals between the Gold chip and the Silver chip. These signals are related to the priority chaining inputs, video bus release input, video data strobe and status information outputs.

6.5.1 Priority chaining input

The Gold chip is, in fact, the last stage of object active arbitration. Two inputs indicate the priority of this arbitration. One is the Even Pixel Priority In input EVI and the other is the Odd Pixel Priority In input ODI. When either or both are active LOW, it means that the Gold chip gets the priority and loads contents in the Background register into the line buffer instead of receiving data from the Silver chip(s). The Background register is a 8 bit register which contains information for both even pixel and odd pixel. For instance, when the inputs EVI is LOW and ODI is HIGH, the Gold chip will load content in the Background register into the even pixel position of the line buffer and waiting for the Silver chip supplying the odd pixel data.

6.5.2 Video bus control

To avoid the contention of the Video data bus among the Gold chip and Silver chips, there is an input to the Gold chip to indicate whether the video data bus is released by the Silver chip. This input RRI is connected to the output pin RRO of Silver chip.

In the system application, the Gold chip always gets the lowest priority. In other words, if there are two Silver chips and one Gold chip serially chained together, the Gold chip will have the lowest priority. When the higher priority Silver chip does not need to access the video bus, it will pull down the chain connected to the second priority Silver chip. If the second priority Silver chip does not use or finishes using the video data bus, it will pull the chain to the Gold chip. Once this input RRI is LOW in the Gold chip, the Gold chip can access the video bus if it needs to.

This chain will be reset HIGH when both even and odd pixels are strobed into the line buffer.

Video data strobe signals includes the Even pixel Video Data Strobe EVDS and Odd pixel Video Data Strobe OVDS They are mainly used for strobing video pixels into the the line buffer by Gold and Silver chips.

Whenever the video pixel data is valid in either Gold and/or Silver chip and ready to be strobed into the line buffer, the video data strobe signal (EVDS or OVDS) will be pulled to active LOW. If both Strobe signals are LOW, an internal video data strobe signal is created and both the Even and Odd pixels are latched into the line buffer.

These two video data strobe signals are bi-directional. The signals are input or output in the Gold chip depending on the signal level of the Priority chain inputs EVI and ODI. Only if the signal level of any Priority chain input is LOW, the video data strobe related to that priority chain input will be swapped to be an output. After both Strobes are asserted to be LOW, these Strobe signals will be swapped back to be inputs by the Gold chip.

For example, if the Even priority input EVI is LOW and the Odd priority input is HIGH in the Gold chip, the Gold chip will load the content of the Background register into the line buffer and asserts the EVDS to active LOW output. Meanwhile, the Gold chip waits for the OVDS active LOW signal. As long as both video data strobes are LOW, the video data (two pixel) will be latched to the line buffer. Then the pixel counter for line buffer is incremented for one count.

6.5.3 Status line outputs

The Gold chip has three status line outputs to provide information to the Silver chips. These three lines are S0, S1 and S2 which can be decoded into eight different conditions. By using this information, the Silver chip can perform some actions such as fetching pixels or loading parameters in the correct sequence.

The following table gives the decoding information of three status line outputs:

S2	S1	S0	Status Description
0	0	0	Refresh Active
0	0	1	No operation
0	1	0	Abort memory cycle
0	1	1	Reset
1	0	0	Top of screen in Even field
1	0	1	Top of screen in Odd field
1	1	0	Pixel Active
1	1	1	Link Load Active

In general, the whole scanning time of a horizontal scan line can be divided into three active intervals. They are "Refresh Active", "Pixel Active" and "Link Load Active".

The "Refresh Active" means the memory system is refreshed during this interval. This Refresh active interval starts right at the falling edge of the Horizontal Sync. The duration of this interval is approximate 10 Gold clocks cycles. During this interval, the Gold chip provides memory refresh address and refresh initiating signal AS (Address Strobe) to the external memory refresh circuit. Then the memory refresh circuit will generate Row Address Strobe RAS and respond with an DAData Acknowledge. The Gold chip will provide five memory addresses sequentially during the entire Refresh Active.

The "Pixel Active" means that the Silver chip can access the memory system and fetch the pixel data. This pixel Active interval starts right after the Refresh Active. The duration of this interval is not fixed and depends on the complexity of the object. In other words, the whole duration is counted on how much time spending on fetching the pixel (the number of memory cycles). Therefore, the Gold chip has pixel counter to calculate time of this interval. At the beginning of this interval

the counter is reset. Then each time when both video data strobes occur (both active LOW) to the line buffer this counter will be incremented. Once the counter reaches 640, the status will be changed to the "Link Load Active". If the counter has not reached 640 but this scan line has run out of time, the Gold chip generates Line buffer incomplete interrupt to CPU. Meanwhile, a new scan line starts and the status will be changed to Refresh Active.

The "Link Load Active" means that the Silver chip can access the memory to load a new Parameter Block. This Parameter Block is described in the Rainbow Silver chip specifications. The duration of this interval depends on the duration of preceeding interval Pixel Active. Obviously, the whole duration can be more than several words memory fetch time or less than one word memory fetch time. Therefore, the Silver always makes sure status lines S0 to S2 stay on Link Load Active before it performs a parameter load memory cycle.

It is very likely that the status is changed back to the Refresh Active during the last parameter fetch. So, the Gold chip will not perform the memory refresh cycle until the Silver chip finishes the present memory cycle. The Gold chip will look for the input pin RRI high to do the memory refresh.

The "Abort Memory Cycle" means that the Gold chip receives a bad memory address detect signal provided by the external "bad address detector" through the RESET input pin. This detect signal is shorter than the regular Reset signal. The details will be explained in the Miscellaneous Control section. When the Silver chip receives this status, it aborts the present memory fetch cycle. The duration of this Abort Memory Cycle is one clock long.

The "Reset" means that the Gold and Silver chips have to reset all registers, counters and state machines. The duration of this interval is three clocks long.

The "Top of screen in Even field" or "Top of screen in Odd field" indicates that the Gold chip is going to display the Even lines or Odd lines. This status occurs after Refresh Active status and at exact two lines before the data actually displayed on the CRT. The duration of this intervalis one clock long.

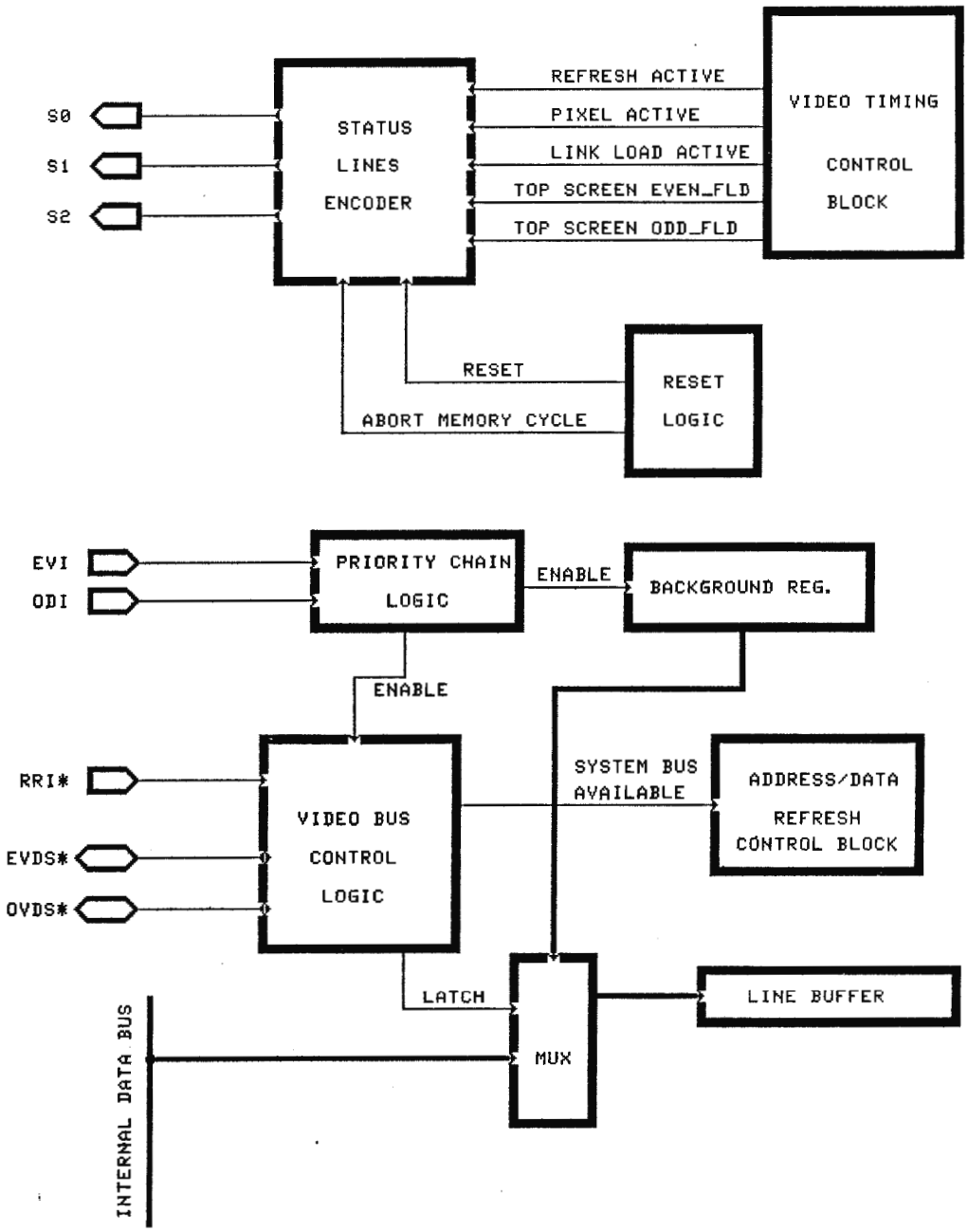
During the video pixel loading period (i.e. from one scan line before starting the display to one line before ending the displya on CRT), the correct sequence of status generated by the Gold chip in order are Refresh Active, Pixel Active and Link Load Active. When loading of Line buffer is incomplete, then status only occurs Refresh Active and Pixel Active.

During noloading of video pixel period (i.e. a whole field period minus the pixel loadine period), the correct sequence in order is Refresh Active , then Link Load Active. However, at two scan lines before data actually displayed on CRT, the Gold chip inserts the Top of Screen in (Even or Odd) field status between Refresh and Link Load Active statuses.

When the Gold chip receives either bad address or Reset signal from outisde, it will generate corresponding status at any time during a scan line.

The block diagram of this Video Data Control logic circuits is shown in the Figure 11.

Figure 11. The block diagram of Video Data Control circuits.



6.6 Address/Data/Refresh control

The Gold chip has a time multiplexe address/data bus to interface with system bus and another 8 bits wide address bus to interface with the Color Map chip. In addition, the Gold chip will provide the refresh address to the memory system during the Refresh Active interval. CPU uses the address/data bus to access the programmable registers or the Color Map chip. During refresh, the Gold chip behaves as another master in the system.

6.6.1 System bus hand-shaking control

The Gold chip provides two hand-shaking control signals. The input is the Processor Request PR and the output is the Processor Grant PG.

Whenever CPU wants to access the programmable registers in the Gold chip or the Color Map it will send a Processor request to the Gold chip. This request signal is initiated by the CPU and created by a bus controller. Once the Gold chip receives this active Low PR signal, the Gold chip will grant the system bus to CPU by pulling Process Grant (PG) Low. If the Gold chip is in the process of a memory refresh cycle, it will finish the cycle then grant the bus to CPU.

6.6.2 System bus address/data interface

The Gold chip provides eleven address lines A0 to A10 and ten data lines D0 to D9 to interface the system bus. These lines are used by CPU to access the programmable registers or the Color Map chip. The Gold chip refreshes memory with these lines.

When CPU wants to access any programmable register in the Gold chip, it will send the Processor Request PR to the Gold chip. After the Gold chip sends back the Processor Grant PG signal to CPU, it will wait for the Address Strobe AS to active LOW then latch the address. Next, the Gold chip will wait for the Write Data Strobe WDS to be LOW then strobe the data into the register. Finally, the Gold chip assert the Data Acknowledge DA to High to inform CPU that data is stored in the register. Figure 12 shows the state machine of writing the Programmable register and Figure 13 shows the timings diagram.

Figure 12. The state machine of Programmable register writing.

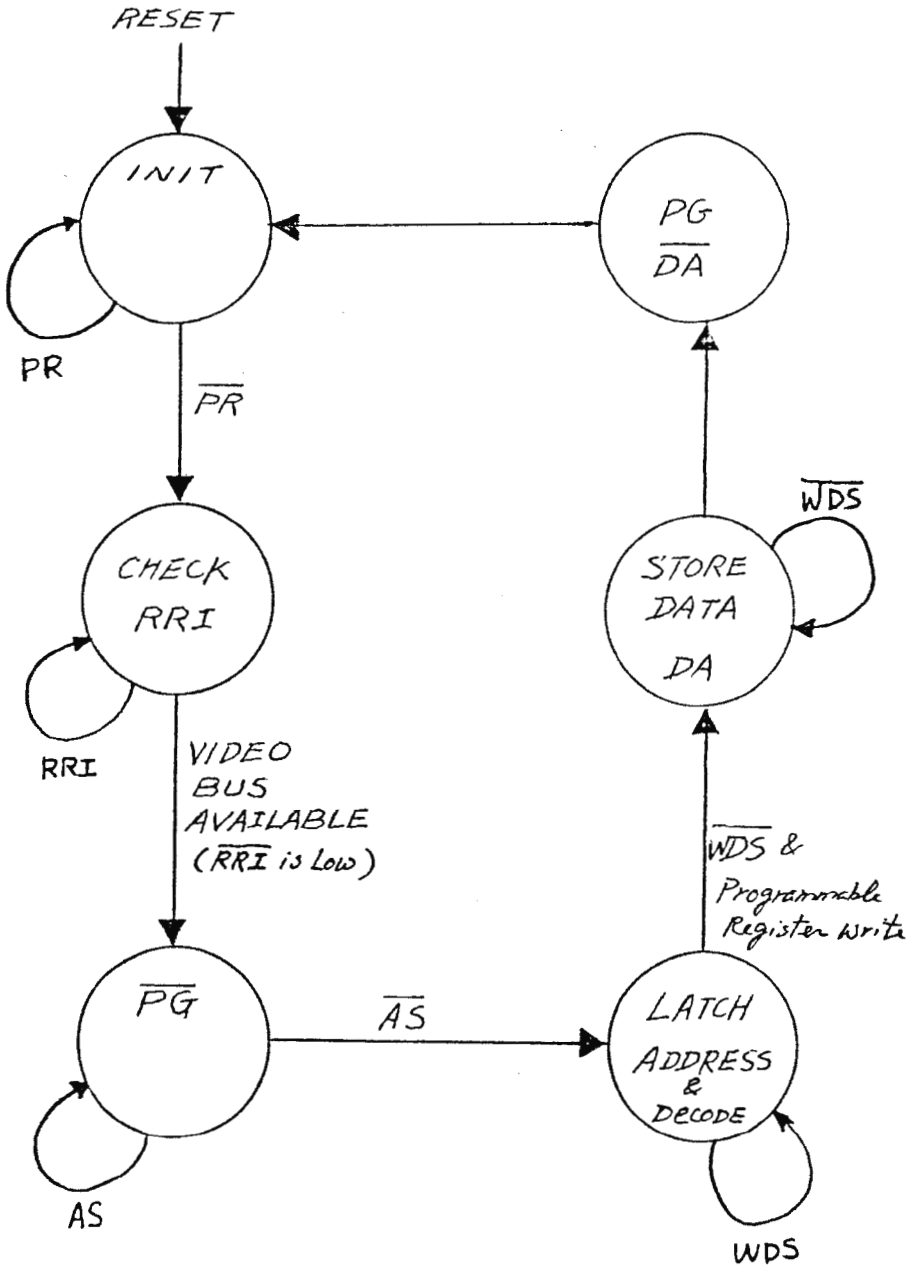
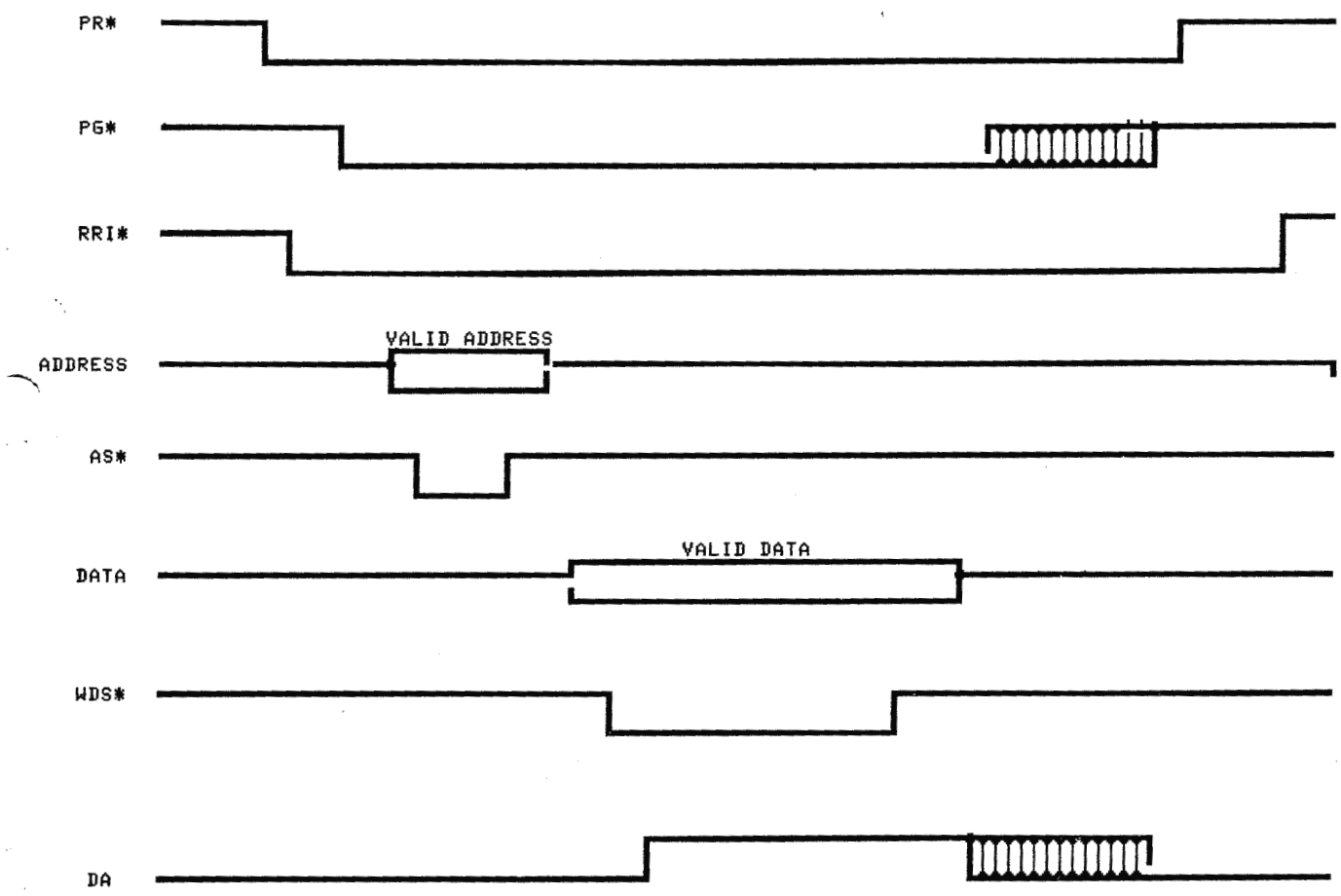


Figure 13. Timing diagram of Programmable Register writing.



When the Gold chip refreshes the memory system during the Refresh Active period (i.e. status lines S0 to s1 indicate the Refresh Active), the Gold chip has to make sure that the input pin RRI is LOW and then assert the Address Strobe AS and place the addresss on the bus One half clock later, the Data Strobe signal is asserted LOW. Next, the Gold chip waits for the Data Acknowledge DA signal back. Once the DA is received High, the Gold chip will start another refresh cycle. The refresh cycle will be repeat five times before the Gold chip change its status to pixel Active.

The state machine of the memory refresh cycle is shown in the Figure 14 and the timing diagram of this cycle is shown in the Figure 15.

6.6.3 Color map address/data interface

When the Color Map is addressed by CPU, the Address Strobe AS is asserted LOW, the input address will be decoded and enable the route from input address lines (A1 to A8) to the Color Map Address output lines (CMA0 to CMA7). Next, the Gold chip waits for the Write Data Strobe WDS to be LOW then asserts the color map write CMWR to LOW. One clock later the Data Acknowledge DA will be asserted to LOW. Meanwhile, the route from input address to the color map output address will be disabled.

The state machine of color map access is shown in the Figure 16 and the timing diagram is shown in the Figure 17.

Figure 14. The state machine of memory refresh cycle.

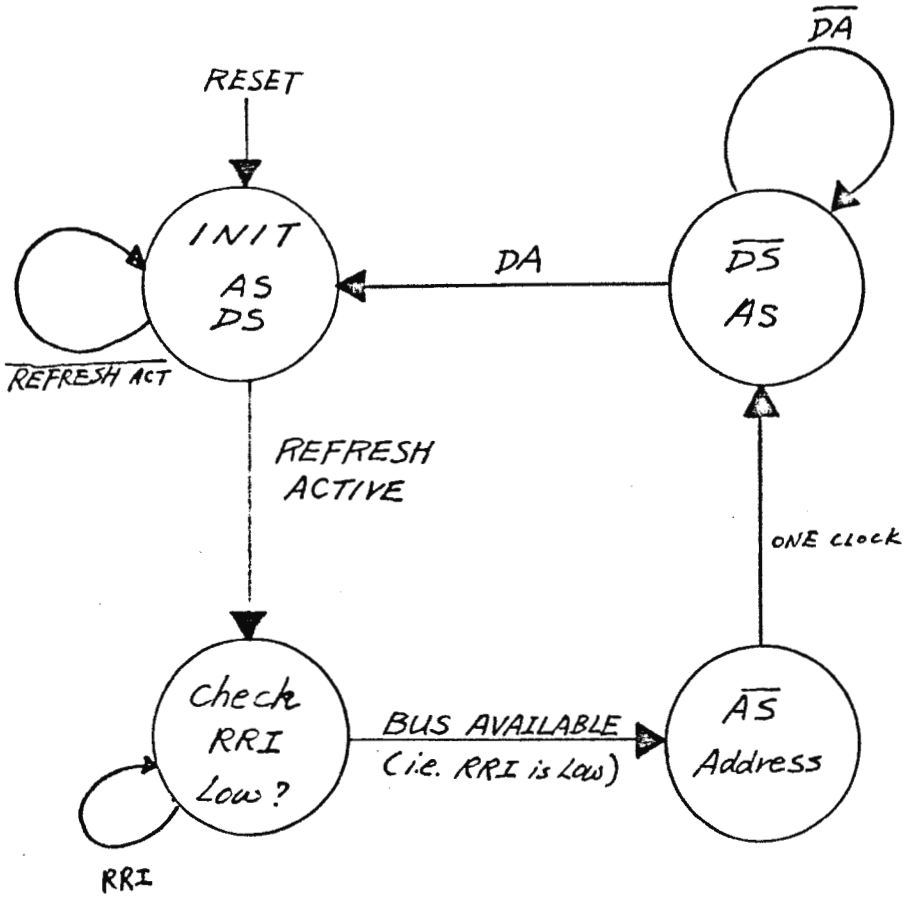


Figure 15. Timing diagram of memory refresh cycle

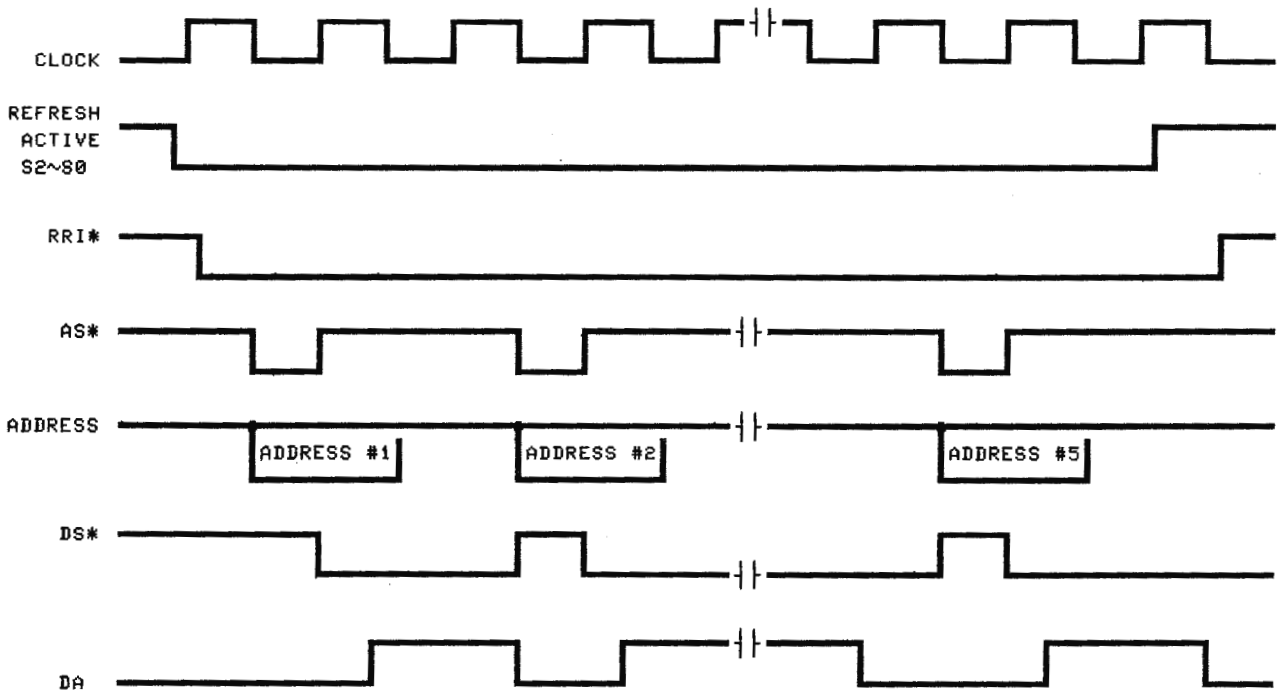


Figure 16. The state machine of color map addressing.

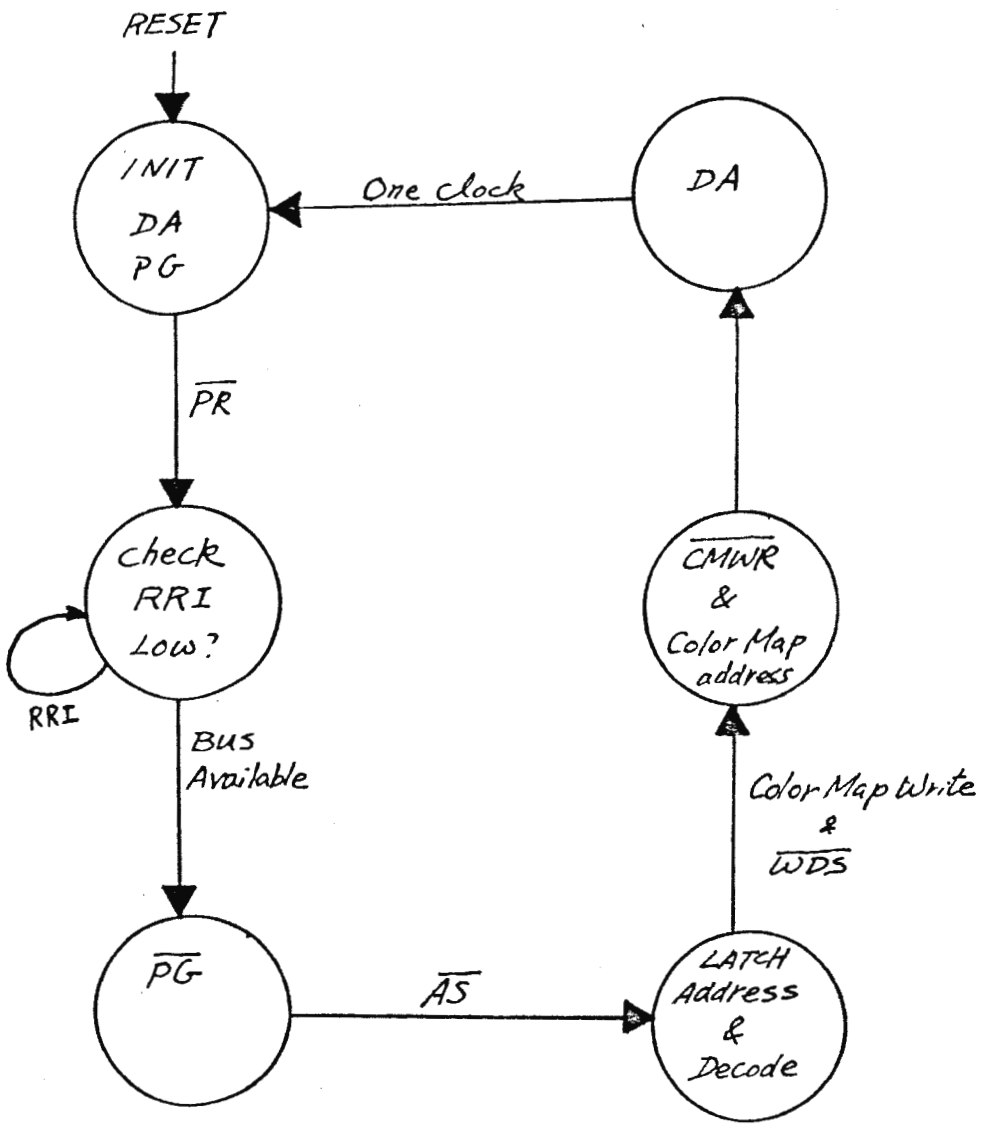
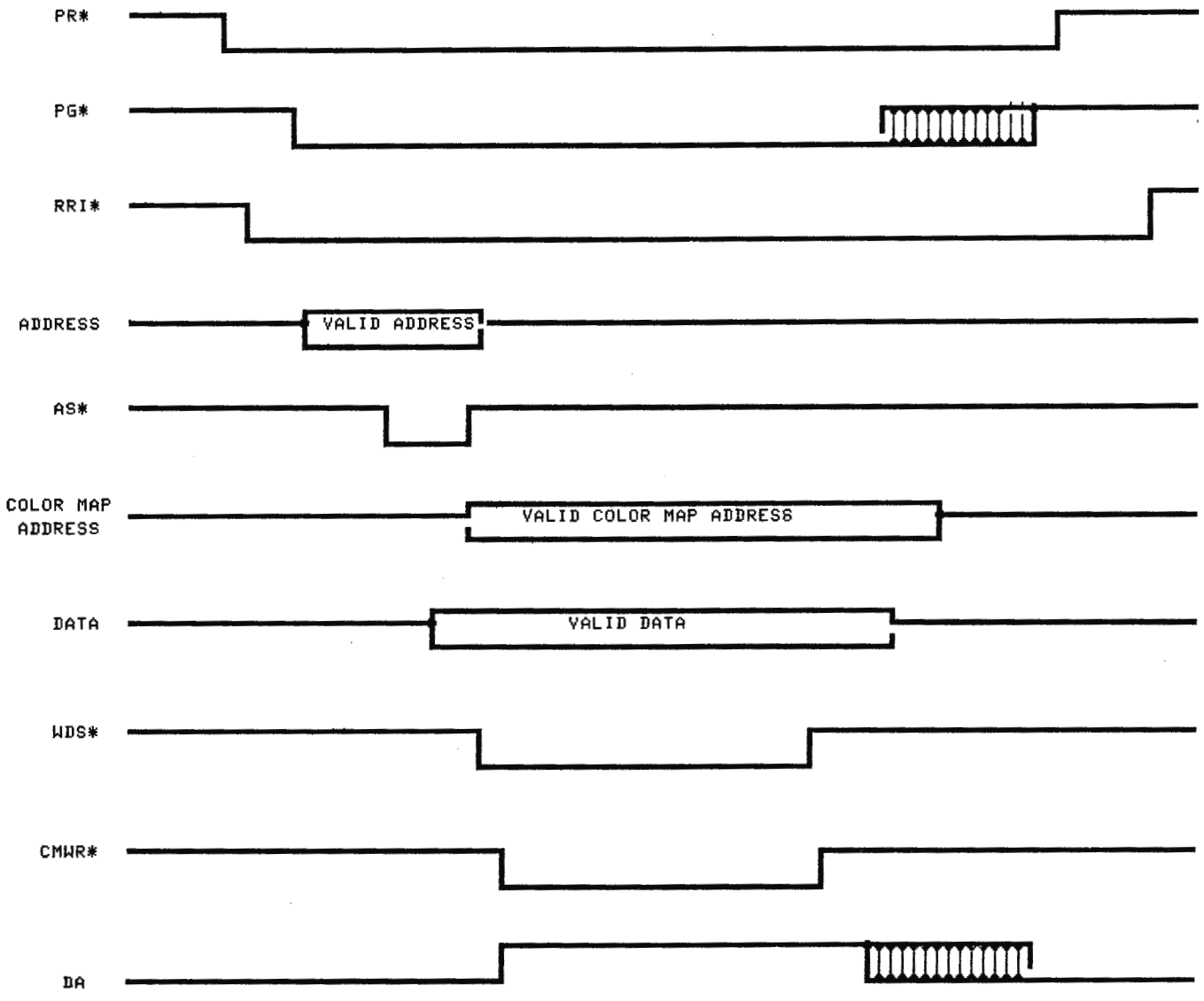


Figure 17. Timing diagram of color map addresssing



6.7 Line buffer and Line buffer control

The line buffer is the place to store the video pixels strobed from the Silver chips and ship out to the Color Map chip one by one in the 12 MHz colock rate.

This line buffer can be thought as a long line buffer with 16 bits in width and 581 bits in length in an conceptual way. In reality, this long line buffer is designed as an dynamic Ram array which is 32 bits in column and 291 words in row.

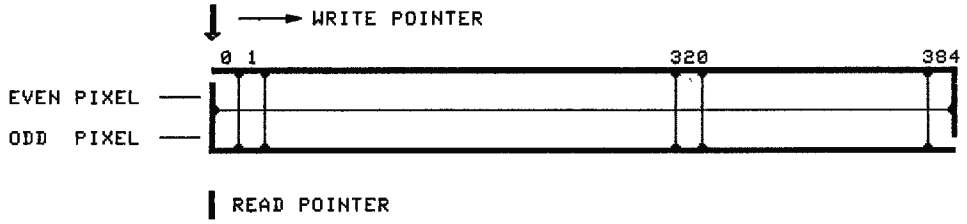
However, it is easy to explain the operation by using a long buffer instead of a Ram array. There are two pointers points to the starting positions of operation in the line buffer. One is the "Read Pointer", the other is the "Write Pointer". At the beginning, both pointers point to the poistion 0. When the video pixel data of the first display line is stored in the line buffer, the Write pointer starts to move to higher position. Whenever a pair of pixels is stored, the Pointer move upward one position. If the Gold chip is programmed to display 640 pixels (which is the fixed number 512 plus the value in the Horizontal Active Video Extension register) in one line, the Write Pointer will stop at position 320 when one whole line is finished. Then the Gold chip ship the pixel data out one by one and the Read pointer moves upward from position 0 to position 320. Meanwhile, the Gold chip continue to fill data in the Line buffer from position 640 upward. When it reaches to the end of the Line buffer, the Write Pointer switches to the position 0 and continue to move upward. This Line buffer can be thought as a cyclic line buffer.

Figure 18 demonstrates this Line buffer in conceptual way.

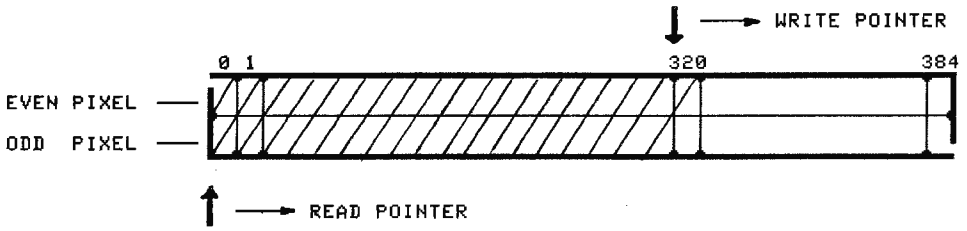
There is a chance that within a line time that the Silver chip can not fill pixels in the Line buffer as programmed number. This could be the case that too many objects overlap together in a one line. Therefore, the Gold chip provides a counter to count how many pixels have been stored in the Line buffer. If the counter reaches the number as programmed, say 640, within a line time, the Gold chip will think a line is completely store in the Line buffer and the status lines (S2 to S0) would change from "Pixel Active" to "Link Load Active". If the counter has not reach 640 (just an example) at the end of a line (Video timing control will provide this signal) then the Line buffer control block generates a "Line buffer incomplete" signal to the Interrupt control block and set the corresponding bit in the Interrupt Status register.

Figure 18. Conceptual descriptions of Reading and Writing of Line buffer.

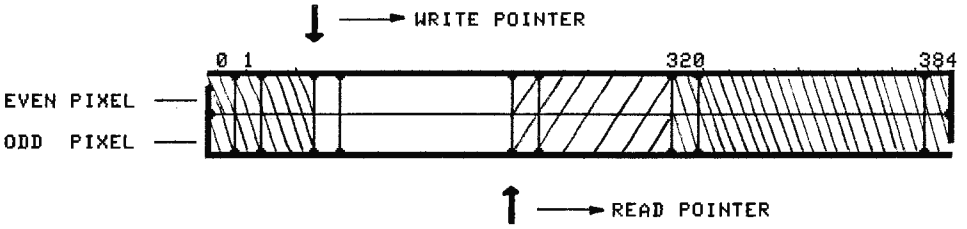
1. AT BEGINNING, NO DISPLAY AND START TO FILL THE FIRST LINE.



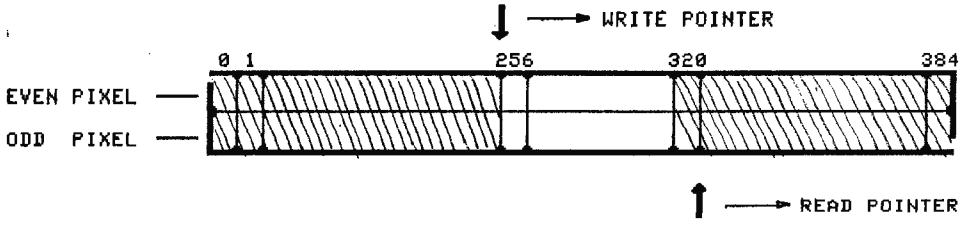
2. START TO DISPLAY THE FIRST LINE AND FILL THE SECOND LINE.



3. IN THE MIDDLE OF DISPLAYING THE FIRST LINE AND WRITING THE SECOND LINE.



4. START TO DISPLAY THE SECOND LINE AND FILL THE THIRD LINE.



In the line buffer incomplete case, the Gold chip still read data from this incomplete line buffer until the Read Pointer stops at the position where the last two valid pixels stored. After that position the Gold chip will send "Blank data" to to the Color Map chip until the total shipped out data is equal to the number as programmed. Meanwhile, the line buffer is filled for next line data.

In terms of hardware design, the Line buffer is a dynamic array. There is a four-pixel latch located in the input of Line buffer and a two-pixel latch located in the output of Line buffer. Every time the Silver chip write a pair of pixels into this input latch. When there are four pixels in the input latch, these pixels then are stored in the buffer. Every time Gold chip reads two pixels into the output latch but ships out one pixel in the one clock period. The whole operation has to synchorize with clock. The reading and writing operation are mutual exclusive.

Figure 19 shows the the basic logic diagram of line buffer and Figure 20 gives the block diagram of Line buffer and line buffer control.

Figure 19. basic logic diagram of line buffer.

Figure 20. The block diagram of the Line buffer and Line buffer control.

6.8 Color Map

Colors to be generated by rainbow are stored in a 256-location memory called the "Color Map" which is a separate chip in the Rainbow system. Thus a Rainbow screenful can have up to 256 distinct colors (unless the CPU reloads the color map within a field).

Color Map is a high speed static Ram with eight address lines and twelve data input/output lines. Each location contains twelve bits of color information so that the total range of the accessible colors is 4096. Four bits data in the color map specify the level of each of read, green and blue. Shades of gray will be generated by equal values for each color, giving 16 gray levels (including black and white levels).

The color map holds, besides the color values, 4 bits in each location for flags. One of the flag bits is to be used by external circuitry to be enable external video data, so that Rainbow-generated and external images (from a video disk, for instance) can be combined on a pixel-by-pixel bais. Other flags may be used to enable external texture-generation signals or smoothing filters.

Other encodings of color values are possible, and Rainbow does not prevent their use. The choice of color and flag encoding will be made by systems designer, will be based on the relative virtues of each encoding (performance, ease of manipulation, and compatibility).

The color map bit allocations are:

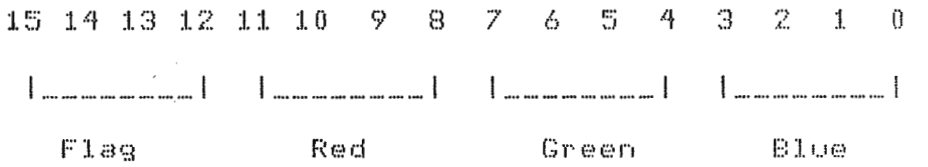
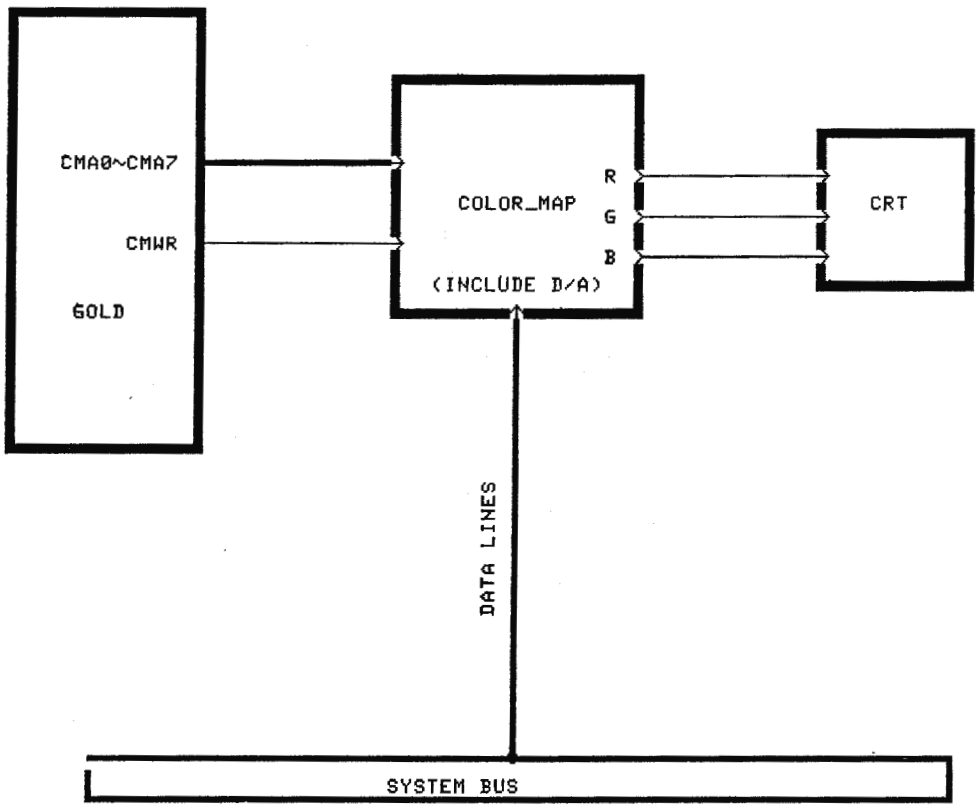


Figure 21 shows the system connections among the Gold chip, Color Map and CRT.

Figure 21. System connections among the Gold chip, Color Map and CRT.



6.9 Miscellaneous control

6.9.1 Reset control

The Gold chip provides a pin RESET for the external system to clear all counters and initialize all registers and registers in both silver chips.

When the RESET input is high, it causes the Gold chip to immediately terminate the present activities. This signal must be active HIGH for at least 10 clock cycles. Meanwhile, the Gold chip will inform the "reset" condition to the Silver chip through the Status bits S0, S1 and S2. The code is described the Status line output section.

Figure 18 shows the internal timimg diagram.

6.9.2 Abort memory cycle control

During the pixel active interval, the Silver chip can access one Mega of bytes memory to fetch the pixel data. If the memory system contains physical memories less than one Mega bytes and the Silver chip accesses a nonexistent or "bad address" location, the Silver chip will never get a Data Acknowledge DA signal from the Memory system. If a DA is never asserted, the Silver chip will be held in a memory cycle indefinitely.

In order to break out of this situation, the Rainbow chip set need an external timer/logic circuit to detect this problem and send a signal to inform the Gold chip. a short pulse (3 to 10 clock cycles) on the RESET pin will cause an Abort status to occur.

After the Gold chip receives this signal from the RESET pin, it measures the period of this signal. If the interval is longer than 3 clock cycles and shorter than ten clock cycles, the Gold chip generate the Status code to the Silver chip. Once the Silver chip receives this status, it will discard the present memory cycle and proceed next operation. Meanwhile, this bad address control block will inform the Interrupt Control block block to interrupt CPU if this condition is not masked.

For each memory cycle, the external logic circuit will be ignited by the Address Strobe AS from the Silver chip and terminated by the Data Acknowledge DA from the memory system. If the timer running excedes a certain amount time(which is assigned by the system designer), then this logic circuit will generate the Abort memory cycle signal.

Figure 22 shows the timing diagram. The system connection between chips and the external logic circuit is shown inthe Figure 23.

Figure 22. Timing Diagram for Reset and Abort Controls

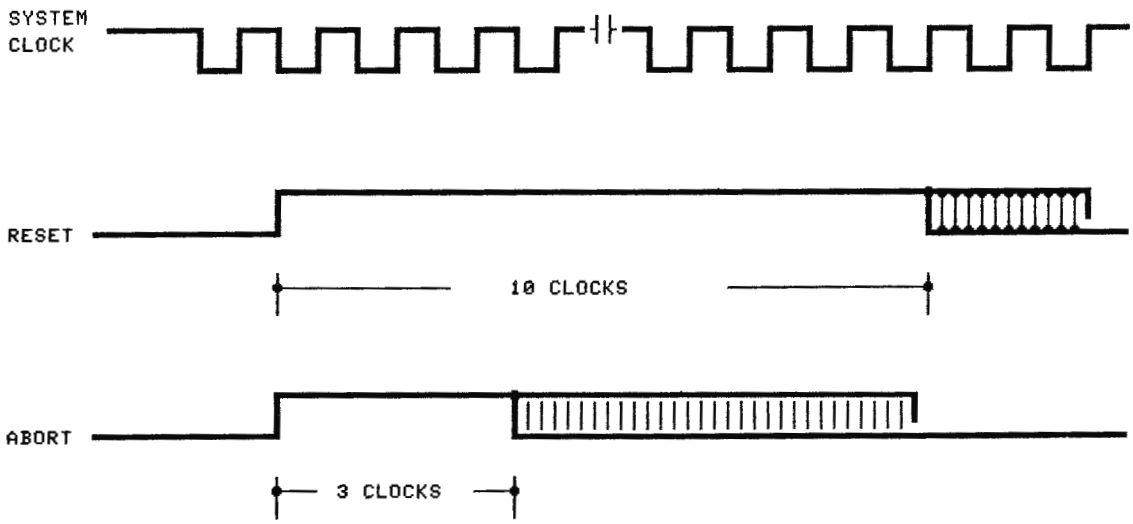
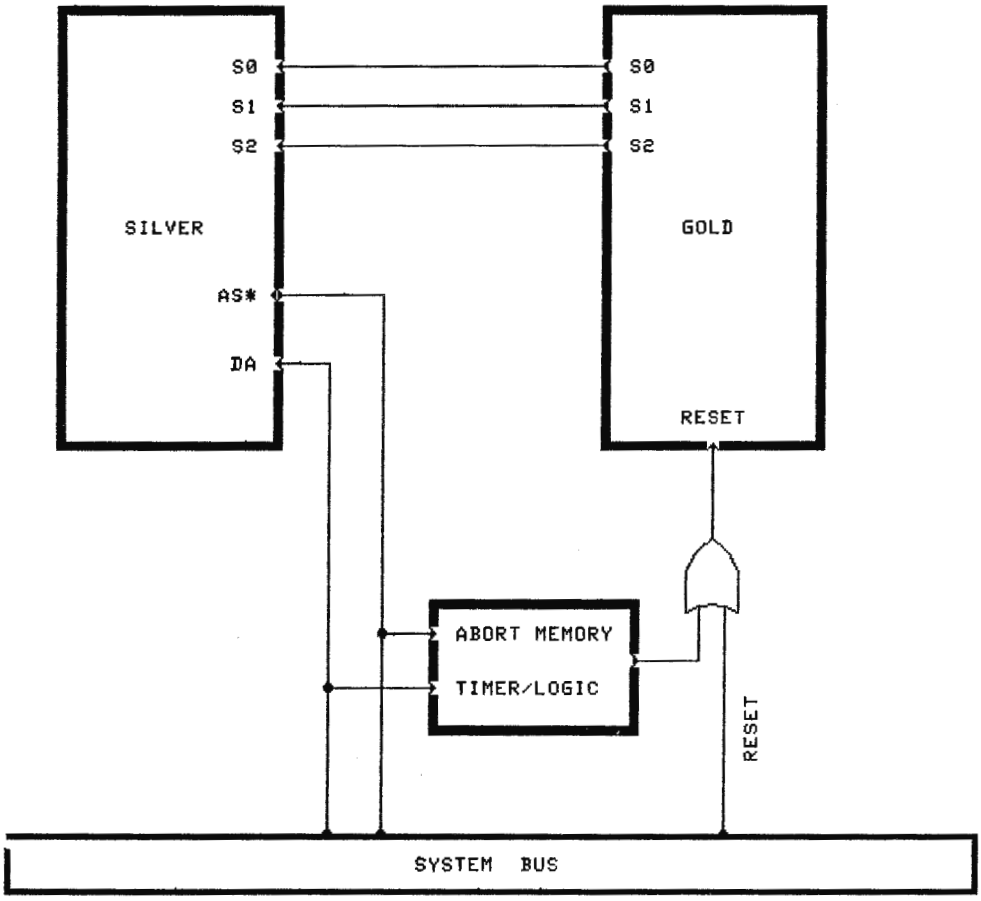


Figure 23. System connection between chips and external timer



6.10 Rainbow system configuration

The minimal Rainbow system is made from two chips Silver and Gold. The Silver chip contains circuitry to read pixel data from memory, process the information and then send the data to ghe Gold chip. The Gold chip provides circuitry forthe video timing, interrupt, programmable registers and line buffer. In addition, several logic circuits are needed by Rainbow system to interface with system bus and CPU.

Figure 24 shows the relationship of the Silver chip and Gold chip with the Color Map, CRT and System bus.

The "Interface Logic" in the figure 24 is a logic circuit that takes care of System Bus request and grant for the Rainbow system.

The "Address/Data buffer" is used for interface between the address/data lines of System Bus and address/data lines of Rainbow system.

The "Bad Address Timer" is a timer to detect a bad address memory access. This timer can be designed to use Address Strobe AS to start counting and Data Acknowledge DA to stop counting. If the counting exceeds a certain value (which is designed by user), then the timer will generate a signal to the Gold chip.

The "Bus Arbiter" takes access request from CPU and generate Processor Request to Rainbow system. Also it performs Bus arbitration between CPU and Rainbow system.

How to implement these Logic circuit depends on what kind of system that the Rainbow system wii fit in.

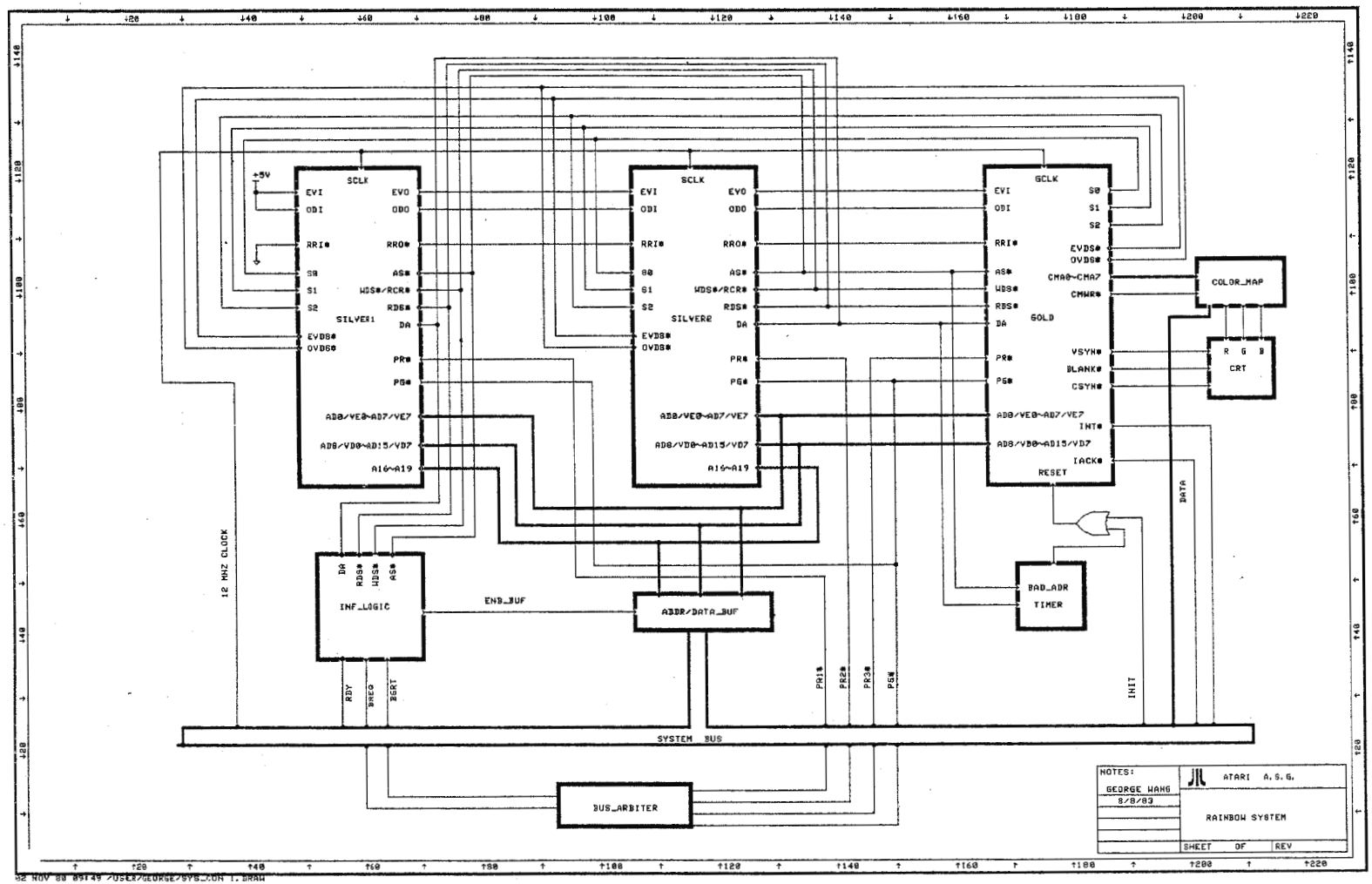


Figure 24. Rainbow system configuration.

1

7. REGISTER ORGANIZATION

The Gold chip contains twelve programmable registers which occupies byte addresses from 512 to 535. These registers can either be readable, writeable or read/writeable. Figure 25 shows the organization of these programmable registers.

7.1 Bit description

Background register

Rainbow generates a background color if no object is displayed This register contains 8 bits data which acts as an indice into the Color Map. The addresses of this register are 256 and 257 for low and high byte data respectively. This register is read/writeable.

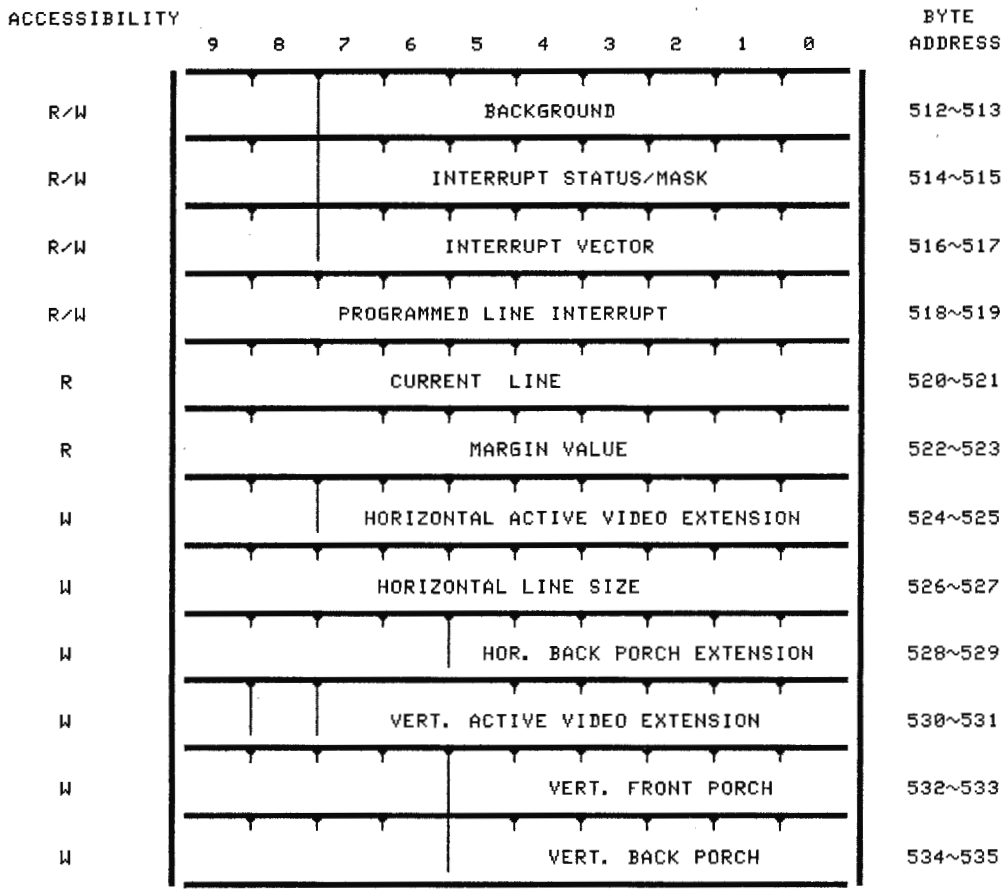
9	8	7	6	5	4	3	2	1	0
		BK7	BK6	BK5	BK4	BK3	BK2	BK1	BK0

Bit	Mnemonic	Description
9-8		not used.
7-0	BK7-BK0	Background register bit 7 (BK7) is the most significant bit and BK0 is the least significant bit in the register.

Interrupt Status/Mask Register

Part of this register is used for masking the interrupt condition. By setting a bit in any three least significant position in register, the corresponding interrupt condition will not occur on the interrupt pin. Part of this registeris used for storing the interrupt status if the occuring interrupt condition is not masked. This register is read/writeable. the addressesof this register are 258 and 259 for low and high byte data respectively.

Figure 25. Register Organization Diagram



** R/W = READ/WRITEABLE

** R = READABLE

** W = WRITEABLE

Bit	Mnemonic	Description
9-8		not used.
7	IS2	Interrupt Status bit 2 (IS2) is used to indicate the Bad Address interrupt condition.
6	IS1	Interrupt Status bit 1 (IS1) is used to indicate the Buffer Incomplete interrupt condition.
5	IS0	Interrupt Status bit 0 (IS0) is used to indicate the Programmed line interrupt condition.
4-3		reserved.
2	IM2	Interrupt Mask bit 2 (IM2) is for masking the Bad Address interrupt.
1	IM1	Interrupt Mask bit 1 (IM1) is used for masking the Line Buffer Incomplete interrupt.
0	IM0	Interrupt Mask bit 0 (IM0) is used for masking the Programmed Line interrupt.

Interrupt vector register

The interrupt vector register is a 8 bit register which is programmed by the user to "OR" with a predefine value to generate the interrupt vector on the data bus line when a interrupr condition occurs. The addresses of this register are 516 and 517. This register is read/writeable.

9	8	7	6	5	4	3	2	1	0
		IV7	IV6	IV5	IV4	IV3	IV2	IV1	IV0

Bit	Mnemonic	Description
9-8		not used.
7-0	IV7-IV0	Interrupt Vector bits; IV7 is the most signicant and IV0 is the least sinificant bit.

Programmed line Interrupt register

The CPU can be interrupted on any specified number in this Programmed line interrupt register. The maximum number of this register depends on the sum of scanning lines in the vertical active video interval and scanning lines in the blanking interval. This number is in the range of 512 to 700 lines.

Because of interlace, the programmed line interrupt will occur on the specified line in the even (odd) field if that line is even- (odd-) numbered, and on the next (line number one greater) line in the odd (even) field. This register is read/writeable and its addresses are 518 and 519.

9	8	7	6	5	4	3	2	1	0
LI9	LI8	LI7	LI6	LI5	LI4	LI3	LI2	LI1	LI0

Bit	Mnemonic	Description
9-0	LI9-LI0	Programmed line interrupt bits; LI9 is the most significant bit and LI0 is the least significant bit. The programmed line interrupt will occur at the beginning of the specified line.

Current line register

Rainbow maintains a read-only location that gives the current line number when read. The line number counts lines to frame, that is, even number on even fields, odd number on odd fields, and continues counting through the blanking time (i.e. it is reset only when a field is about to begin). This register provides some software uses such as it tells how many line times remain in the blanking time. This register is readable and its addresses are 520 and 521.

Bit	Mnemonic	Description
9-0	CL9-CL0	Current line value register bits. The CL9 is the most significant bit and the CL0 is the least significant bit. The range of the value of this register depends on the sum of scanning lines in the active video interval and scanning lines in the blankng interval.

Margin Value register

As an adjunct to the incomplete interupt, Rainbow keeps a read-only location that tells how much time (measured in pixel clocks) was left when the previous line buffer was completed. This can be used as advance warning of impending incomplete interrupts, or as a measure of the complexity of an image. This location will be zero following a line which causes an incomplete interrupt. This register is readable and its addresses are 522 and 523.

Bit	Mnemonic	Description
9-0	M9-M0	Margin value bits, M9 is the most significant bit and the M0 is the least significant bit. The number could be from 0 to 640.

Horizontal Active video extension register

The horizontal active video part is the interval that contains the display video pixels. This interval is partially programmable. In other words, it will display 512 pixels minimun plus the programmed video pixel extension. The range of of this extension is from 0 to 255. This register is writeable and its addresses are 524 and 525.

Bit	Mnemonic	Description
9-8		not used.
7-0	HAX7-HAX0	Horizontal active video extension bits. The HAX7 is the most significant bit and the HAX0 is the least significant bit.

Horizontal line size register

The horizontal line size describes how many pixel clocks in a horizontal scan line. The main purpose of this vlue is to obtain the half line size which results in getting the right timing of vertical Sync. Obviously, this interval includes the video pixel active displayed interval and the blanking interval. In general, the total number pixel clocks of a horizontal scan line is 512 at least and 1023 is maximum.

Bit	Mnemonic	Description
9-0	HL9-HL0	Horizontal line size bits; the HL9 is the most significant bit and the HL0 is the least the least significant bit.

Horizontal back porch extension register

The horizontal back porch is the number of video pixel delays after the horizontal Sync. This interval consists of regular back porch and back porch extension. The duration of regular back porch is 32 video pixel long and back porch extension can be programmed from none to 31 pixel long. This register is writeable and its addresses are 524 and 525.

The Interval of Horizontal Sync in the NTSC TV system is defined to be a value equivalent to 0.075H (H is the time from start of one line to start of next line).

9	8	7	6	5	4	3	2	1	0
				HBX5	HBX4	HBX3	HBX2	HBX1	HBX0

Bit	Mnemonic	Description
9-6		not used.
5-0	HBX5-HBX0	Horizontal back porch extension bits. The HBX5 is the most significant bit and the HBX0 is least significant bit.

Vertical active video extension & Interlace select mode register

Each video frame contains fixed display active lines and the active video extension part. The duration of this extension can be programmed as short as zero line or as long as 256 lines. In other words, total horizontal scanning lines is from 384 lines to 640 lines. Bit is always zero.

Rainbow Gold will generate interlaced video signals for full vertical resolution on normal (NTSC and monitor) displays. There is provision for use in non-interlaced system. There is a bit in this register for this purpose. This register is writeable and its addresses are 530 and 531.

9	8	7	6	5	4	3	2	1	0
	NIN	VAX7	VAX6	VAX5	VAX4	VAX3	VAX2	VAX1	VAX0

Bit	Mnemonic	Description
9		not used
8	NIN	Non-interlaced mode bit; If this bit NIN is set, the Gold chip will generate even field only.
7-0	VAX7-VAX0	Vertical active video extension bits; The VAX7 is the most significant bit and the VVX0 is the least significant bit. Bit VAX0 is always zero.

Vertical front porch register

The vertical front porch is the number of the horizotal scan line delays before the Vertical Sync. The duration of this interval can be programmed from none to 62 scan lines long. This number is in terms of frame not the field. In other words, this number is always an even number and will be divided by two for each field.

The interval of Vertical Sync in the NTSC TV system is defined as a value of 3H (H is the time from start of one line to start of next line). This register is writeableand its addresses 532 and 533.

9	8	7	6	5	4	3	2	1	0
				VFP5	VFP4	VFP3	VFP2	VFP1	VFP0

Bit	Mnemonic	Description
9-6		not used.
5-0	VFP5-VFP0	Vertical front porch bits; The VFP5 is the most significant bit and the VFP0 is the least significant bit and always is zero.

Vertical back porch register

The vertical back porch is the number of the horizotal scan line delays between the Vertical Sync and the displayed information. The duration of this interval can be programmed from none to 62 scan lines long in terms of frame. This number is always an even number and will be divided by two for using in each field. This register is writeable and its addresses are 534 and 535.

9	8	7	6	5	4	3	2	1	0
				VBP5	VBP4	VBP3	VBP2	VBP1	VBP0

Bit	Mnemonic	Description
9-6		not used.
5-0	VBP5-VBP0	Vertical front porch bits; The VBP5 is the most significant bit and the VBP0 is the least significant bit and always si zero.

8. MAXIMUM RATINGS

Storage Temperature	-65 to +150 C
Ambient Temperature under Bias	0 to +70 C
Voltage at Pin releative to Ground	-0.5 to +7 C
Power Dissipation	750 mW

note: beyond the maximum ratings useful life may be impaired.

9. CAPACITANCES

Ambient Temperature Parameters: T_A=25 C; V_{cc}=GND=0V

Symbol	Parameter	Min	Max	Units	Test Cond.
C_{in}	Input Capacitance		10	$_pF$	
C_{out}	Output Capacitance		15	$_pF$	

10. D.C. CHARACTERISTICS

Ambient Temperature Parameters: T_A= 0 C to 70 C; V_{cc}= +5V +10%

Symbol	Parameter	Min	Max	Unit	Test Cond.
V_{IL}	Input Low Voltage	-0.5	+0.8	V	
V_{IH}	Input High Voltage	+2.0	V_{cc}+0.5	V	
V_{OL}	Output Low Voltage		+0.45	V	
V_{OH}	Output High Voltage	+2.4		V	
I_{IL}	Input Leakage Current		+10	V	
I_{OL}	Output Leakage Current		+10	V	