

ATARI 25601 HARDWARE TECHNICAL SPECIFICATIONS

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Atari, Inc. CONFIDENTIAL  
Trade Secrets Enclosed

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## 1.0 INTRODUCTION

This document is the Technical Specification for the Atari 25601 Home Computer. It will describe the electrical and mechanical features of the machine in detail. It will also detail the software requirements placed on the hardware of the machine. This document will provide references to other Atari documents and non-Atari documents. These references are an integral part of this Technical Specification. This specification also contains a set of appendices that describe suggested methods of implementing some of the technical requirements of the machine.

## 2.0 TERMINOLOGY

A1200  
1200                   Atari 1200XL Home Computer  
1200XL

MS-DOS:               Microsoft Disk Operating System  
                      (Used in the IBM-PC)

IBM Basic A:         Advanced Basic (Used in the IBM-PC)

A-1050:              Atari 1050 Disk Drive

I.C.:                 Integrated Circuit

SALLY:               6502 compatible microprocessor custom to Atari

ANTIC:               Custom I.C.'s used in A-1200 family of  
GTIA:                 computers for display creation.

POKEY:               Custom I.C. used in A-1200 family of computers  
                      for sound generation.

FREDDIE:             Custom I.C. used in A-1200 family of computers  
                      for Dynamic RAM control.

1200XL PRODUCT FAMILY: Series of Atari computers consistent in  
                          architecture and interfaces. This family is  
                          different in some areas from the 400/800  
                          family.

*and exceedingly unpopular because  
of these differences*

IBM PC

IBM Personal Computer Model 5150

[www.atarimuseum.com](http://www.atarimuseum.com)

3.0 REFERENCES

- [ 1] Atari Sweet-16 Home Computer Product Specification
- [ 2] POKEY SPECIFICATIONS (CO12294)
- [ 3] ANTIC SPECIFICATIONS (CO12296)
- [ 4] GTIA SPECIFICATIONS (CO14805)
- [ 5] SALLY SPECIFICATIONS (CO14806)
- [ 6] 6502 DATA SHEET
- [ 7] PIA (6520) DATA SHEET
- [ 8] FREDDIE SPECIFICATIONS
- [ 9] VOTRAX SC-01 DATA SHEET
- [10] IBM-PC TECHNICAL REFERENCE MANUAL (Updated January, 1983)
- [11] ATARI 1050 DISK DRIVE PRODUCT SPECIFICATION
- [12] ATARI 800 HARDWARE MANUAL (CO16555)
- [13] ENVIRONMENTAL SPECIFICATION MANUAL (CO61616)
- [14] RF MODULATOR SPECIFICATION (CO61619)
- [15] RF CABLE SPECIFICATION (CA061177)
- [16] RF SWITCH BOX SPECIFICATION (CA010112)

#### 4.0 PRODUCT FEATURES

The Atari 25601 Computer will be designed to be upward compatible with the current generation of Atari computers (e.g. Atari 1200XL). The level of compatibility with the Atari machines shall allow all Atari 1200XL compatible software programs that use defined operating system entry points to run on the 25601. All Atari Peripherals shall also work with the machine.

The 25601 shall provide the following hardware entities to ascertain the above compatibility requirements.

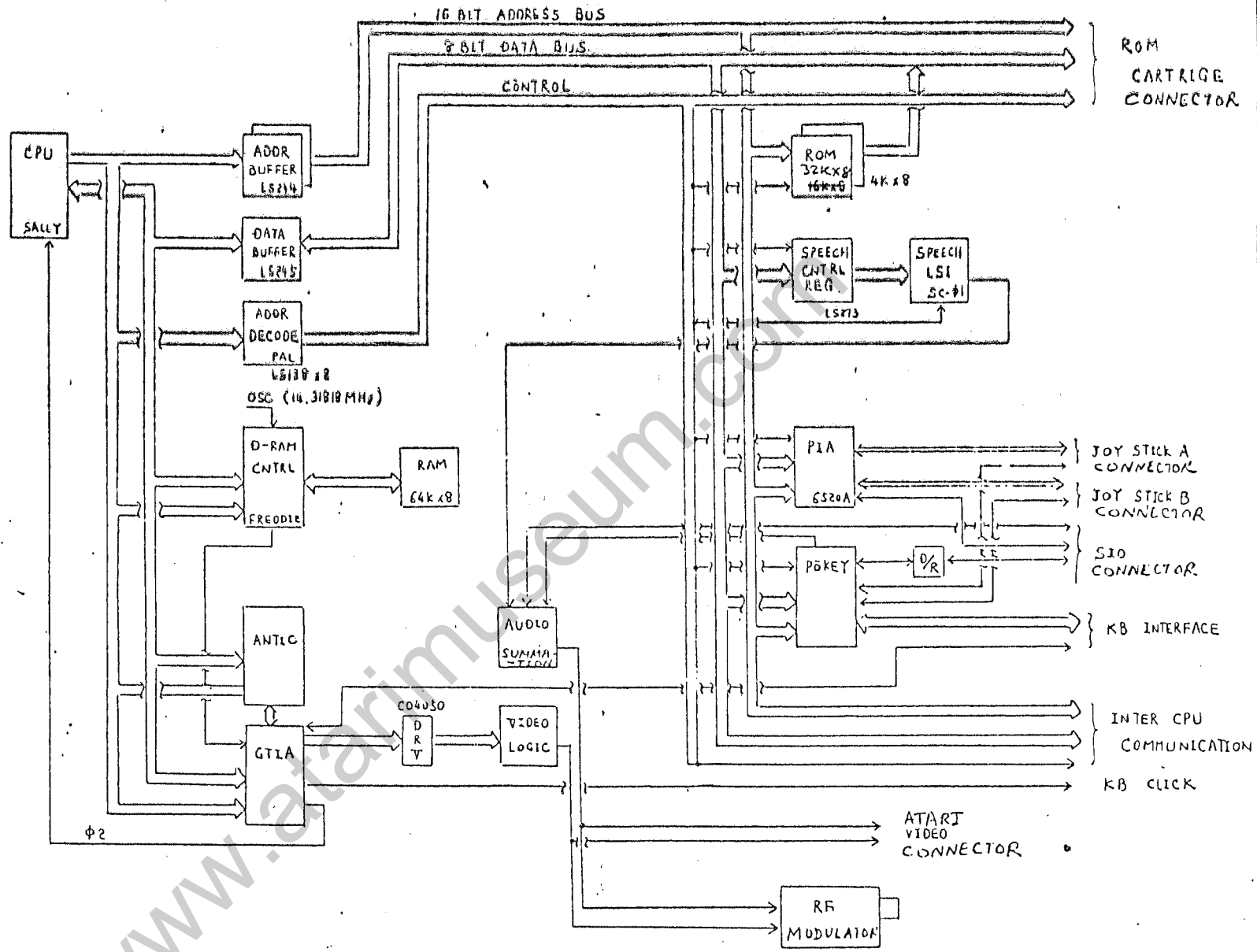
- (a) One A-1200XL Compatible Cartridge Slot
- (b) One A-1200XL Compatible Serial Input Output (SIO) Interface.
- (c) Two A-1200XL Compatible Controller (joystick) ports
- (d) One A-1200XL Compatible Video (monitor) connector
- (e) Keyboard that is upward compatible with the A1200 keyboard
- (f) A built-in disk drive that is upward compatible with the A-1050 disk drive.
- (g) An Atari compatible voice synthesis utility
- (h) An R.F. Out phono connector with channel select for channel 2 and 3.

To meet the above requirements, a portion of the machine's hardware shall have an architecture identical to the A-1200 architecture. (See Appendix 1.1)

The 25601 shall also be designed to be compatible to an extent with the IBM Personal Computer. The level of compatibility with the IBM-PC shall allow all MS-DOS Version 1.25 (PC-DOS Version 1.1) compatible software titles to run unchanged on the 25601. All IBM-PC BASIC-A (Advanced BASIC) compatible titles shall also run unchanged on the 25601 with fully compatible BASIC-A installed. In addition to the above requirements, the hardware and software design of the machine shall attempt to be as compatible as possible with other IBM-PC software. The 25601 will provide the following hardware features to achieve these compatibility requirements:

- (a) Four IBM-PC compatible expansion slots to allow optional hardware to be plugged into the machine.

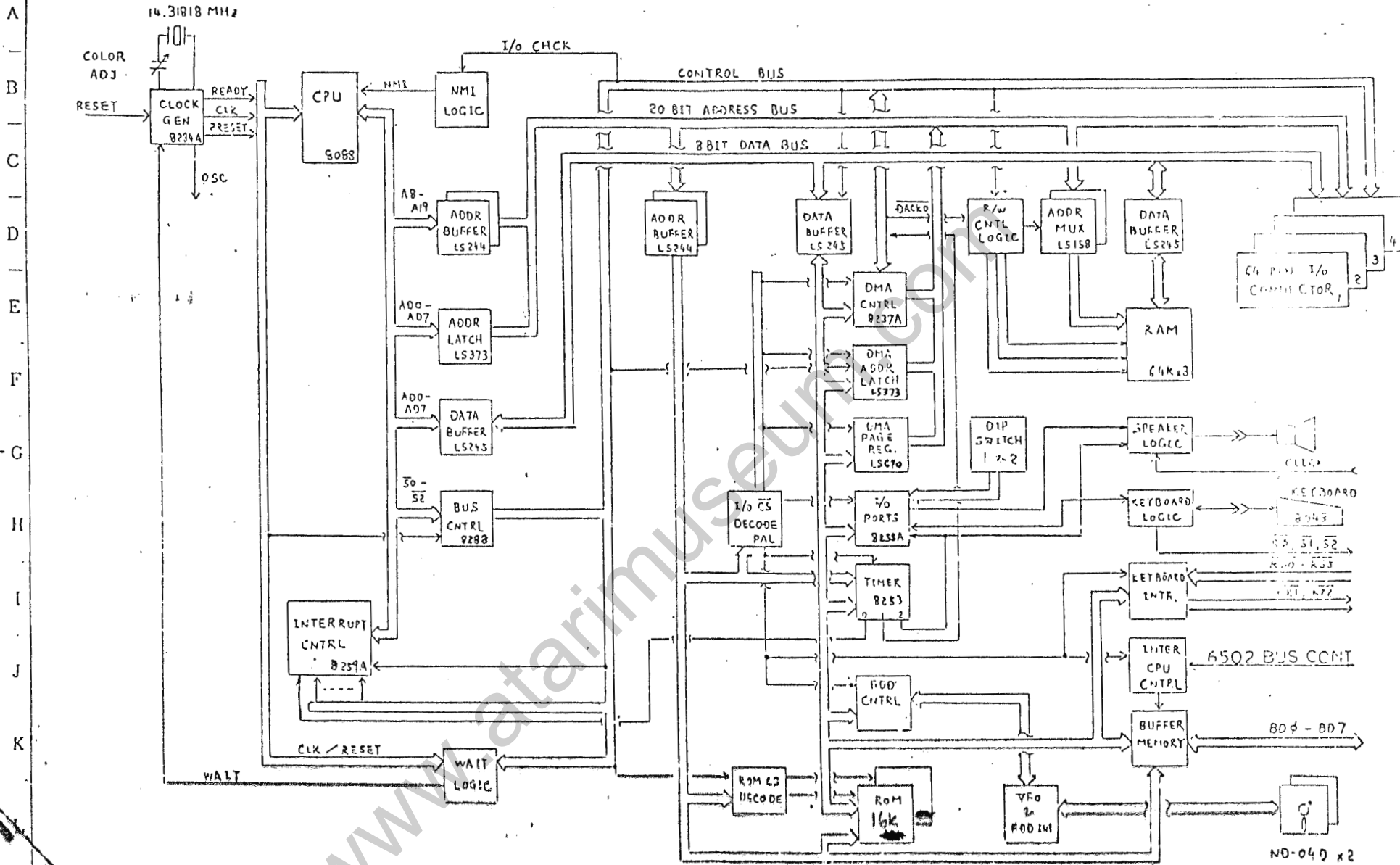




REVISED BY	REVISED DATE	PRINTED BOARD	TITLE ATARI 2601 BLOCK DIAGRAM		
CHECKED BY	DESIGNED BY	DRAWING DATE	SII. No.	DRAWING No.	PAGE No. REV. MARK

FIG. 4.1(a)

NOT RELEASED



NOT RELEASED

DESIGNED BY	REVISED DATE	PRINTED BOARD	TITLE ATARI 25601 BLOCK DIAGRAM	
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1	2	3	4	PAGE No. REV. MARK

FIG. 4.1(b)

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*really, or our "dual" density  
tiny capacity disk?*

- (b) 5 1/4" double sided, double density disk drive that is media compatible with the IBM-PC disk drive. One disk drive will be standard in the machine. Firmware and space will be provided to install a second optional, internal disk drive. The machine will also be designed to provide hardware so that a user can easily install a second optional disk drive. The power supply shall be designed to support this second disk drive.
- (c) The machine will support a detachable full-stroke keyboard having all the keys of the IBM-PC keyboard. The layout of the keyboard shall be identical to the layout of the IBM-PC keyboard. The keyboard will have 3 additional keys to implement the START, SELECT and OPTION functions. (See Sec. 5.1.2.1 for the keyboard layout). See Section 5.1.2.1 for description of the keyboard connector.

#### 4.1 System Architecture

Figure 4.1 is a detailed block diagram of the machines hardware. The 25601 essentially consists of 2 independent computer sub-systems:

- (a) A SALLY based sub-system
- (b) An 8088 based sub-system

These two sub-systems communicate with each other over a well defined interface.

##### 4.1.1 SALLY Sub-system:

The SALLY Sub-system (See Figure 4.1(b)) consists of SALLY, ANTIC, GTIA, POKEY and PIA integrated circuits. A description of these integrated circuits can be found in [2] through [7]. The interconnection scheme of these I.C.'s is described in [1] and in Appendix 1.1.

The SALLY Sub-system includes 64 kilobytes of Dynamic Read Write Memory (DRAM) supported by the "FREDDIE DRAM" D-RAM Control I.C. See [8] for a description of FREDDIE. The SALLY Sub-system also supports the VOTRAX SC-01 [9] based Speech Synthesis I.C. and associated circuitry. The SALLY Sub-system has one 16K ROM I.C. for the SALLY Operating System and one 4K ROM I.C. for software handlers. The Sub-system has circuitry for decoding the address lines and control signals. The decoding circuitry implements the memory map described in Section 5.3.2.3. The SALLY Sub-system contains electronics to interface the RF modulator and the Atari Video Connector to the video and audio signals generated by GTIA and POKEY respectively. The SALLY System also has circuitry to connect PIA and POKEY

outputs to the SIO and controller connectors.

Appendix 1.1 details a suggested and recommended method of implementing the SALLY Sub-system.

#### 4.1.2 The 8088 Sub-System

The 8088 Sub-system consists of the Intel 8088 microprocessor and its supporting I.C.'s (8288, 8284, 8259, 8253, 8255 and 8237). These I.C.'s are connected to satisfy the IBM compatibility requirements of Section 4.0. The 8088 Sub-system supports 64 kilobytes of Dynamic Read Write Memory (D-RAM) on the 8088 bus. The main PCB shall be designed with sockets for an additional 64K of RAM. The system shall be designed so that with a jumper option, the user can configure it to accept 256K X 1 D-RAMs. This will allow the machine to be upgraded to a 512K byte machine on the 8088 side. The machine will also support 16K of ROM on the 8088 bus for the BIOS and device handlers. The 8088 Sub-system provides 4 IBM-PC compatible I/O slots. See [10] for detailed description of these slots. The 8088 Sub-system address decoding circuitry implements the memory map described in Section 5.3.3.4. The 8088 bus also supports a floppy disk controller. This controller and associated circuitry control a built-in disk drive that is capable (under software control) of reading and writing IBM-PC format and Atari 1050 format compatible diskettes.

The 8088 Sub-system includes IBM-PC compatible DIP SWITCHES for Configuration setting. An IBM P.C. compatible speaker is provided. The speaker logic also sums the key-click signal from the GTIA on SALLY side. The keyboard connects to the 8088 side of the machine as shown in Figure 4.1.

The keyboard is a detachable keyboard with connector signals as described in Section 5.1.2.1.

#### 4.1.3 Inter-Sub-System Interfaces

The 8088 System and the SALLY System are coupled through two interfaces:

- (A) The Keyboard Interface: This interface simulates a key-matrix for the POKEY scan lines. The 8088 processor writes into this key matrix under software control. The information in this matrix is subsequently scanned by POKEY. A preferred block diagram of implementing this interface is in Appendix 1.2.
- (B) The Inter-Processor Interface: This interface is

the primary avenue of information exchange between the two sub-systems. The primary use of this interface is:

(i) The SALLY processor shall be able to access the disk sub-system on the 8088 side through this interface. This utility of the interface is further discussed in Section 5.3.

The secondary uses of this interface are as follows:

(i) The SALLY processor shall be able to access the utilities on the 8088 bus (such as the I/O slot devices, the timer device, etc.)

(ii) The 8088 processor shall be able to access the utilities on the SALLY bus (such as the SIO devices, controller ports, speech utility, etc.)

The handler software for the primary use of this interface will be resident in machine ROM. The handler software for the secondary utilities will be loadable optionally in RAM.

Appendix 1.3 details the preferred implementation of the Inter-processor communication interface.

www.atariuser.com

## 5.0 TECHNICAL REQUIREMENTS

### 5.1 ELECTRICAL

The electrical functionality of this machine shall be such that it will run all software designed to run on the Atari 1200 series products with the following exceptions: any software requiring the integral modem, or software requiring the optional parallel bus. The hardware will provide interfaces to one Atari cartridge slot, two Atari controller ports, the Atari SIO bus, a standard NTSC television, and an optional monitor.

The hardware will also provide the necessary circuitry to interface to, up to, two integrated double density, double sided 5-1/4" floppy disk drives. The circuitry will also support, both from a logic and power standpoint, four expansion slots similar to those found in the IBM PC. These slots will be capable of accepting and running cards designed to run in the IBM PC.

The hardware shall also provide the capability for both the 8088 and the SALLY processors to be running simultaneously and semi-independently.

#### 5.1.1 ATARI I/O

##### 5.1.1.1 CONTROLLER JACK INTERFACE

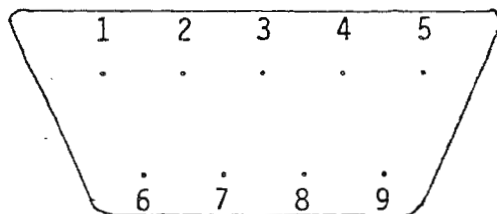
The 25601 provides two controller jack interfaces. Both are functionally and electrically identical. The controller jacks are 9 pin D type male connectors (see Figure 5.2) with the following signals:

PIN 1 thru PIN 4 are general purpose I/O lines. The direction of each of these lines is individually programmable by writing into the PIA internal registers. When a joystick is connected to the controller jacks, these lines are the FWD (Forward), BACK, LEFT and RIGHT inputs respectively, providing direction control inputs to the 25601. See [7] and [12] for discussion on the direction control mechanism for these lines. [12] also describes the configuration of these lines when other input devices such as paddles are connected to these lines.

PIN 5 and 9 are BPOT input and APOT input, respectively. These inputs accept the outputs from the potentiometers in the two paddles that can be connected to the controller interfaces.

PIN 6 is the "active low" TRIGGER input from the controllers eg. joysticks, paddles). These inputs are also

Controller Jack (Looking Into The 25601 Connector)



- 1. (Joystick) Forward Input
- 2. (Joystick) Back Input
- 3. (Joystick) Left Input
- 4. (Joystick) Right Input
- 5. B Potentiometer, Input

- 6. Trigger Input
- 7. +5 volts
- 8. Ground
- 9. A Potentiometer Input

Fig. 5.2

NOT RELEASED

designed to accept the light pen signal. When this line goes low, the GTIA LP (light pen) input is pulled low. See [1] for details.

PIN 7 is the Vcc output to the controllers. This Lower output has a nominal value of Vcc.

PIN 8 is the GROUND reference for the controllers.

#### ELECTRICAL LEVELS

PINS 1 thru PIN 4 are buffered inputs in parallel, with ratioed outputs (with static protection circuitry) and have the following characteristics:

Input 0 level -0.5 Vdc (min) :::: 0.8 Vdc (max)

Input 1 level 2.0Vdc (min) :::: 5.25Vdc (max)

Output 0 level at 1.6mA 0.0Vdc (min) :::: 0.56Vdc (max)

Output 1 level at -100 micro amp 2.4Vdc (min) :::  
5.0Vdc (max)

Capacitance 0.001 micro Farads (max)

Load Current at 2.4Vdc 100 microamps (min)

PINS 5 and 9 are Schmitt Trigger inputs with a low threshold of 1 Vdc (max) and a high threshold of 1.7 Vdc (min) and a hysteresis of 0.3 Vdc (min). The max input capacitance is 15 pF.

PIN 6 has the following electrical characteristics:

Logic 0 Input level 0.8 Vdc (max)

Logic 1 Input Level 2.0 Vdc (min)

Input capacitance 25 pF (max)



### 5.1.1.2 CARTRIDGE INTERFACE

The cartridge interface is a 30 pin 15/30 Dual Readout connector (figure 5.3) with the following pin-out:

PIN 1 is the S4 Select output to the cartridge. This line goes low if the RD4 input (PIN A) is active and an address between 8000H and 9FFFH is involved on the CPU bus.

PIN 12 is the S5 Select output to the cartridge. This line goes low if the RD5 input (PIN 14) is active and an address between A000H and BFFFH is involved on the CPU bus.

PIN A is the RD4 input from the cartridge. If a cartridge uses addresses between 8000H and 9FFFH, it should pull this line high internally. When this line is pulled high, the S-16 maps the address 8000H thru 9FFFH to the cartridge.

PIN 14 is RD5 input from the cartridge. If a cartridge uses addresses A000H to BFFFH, it should pull this line high internally. The 25601 O.S. pulls this line to sense a cartridge. If this line is sensed high, the 25601 maps the addresses between A000H and BFFFH to the cartridge.

PIN 15 is the Cartridge Control (CCNTL) output to the cartridge. This output is pulled low, if an address of the form D5XXH is invoked on the CPU bus.

PIN S is the Buffered Phase 2 (B02) output to the cartridge. The cartridge may use this clock for its internal timing.

PIN R is the CPU Read/Write output to the cartridge from the CPU.

PINS 5, 4, 3, 2, C, D, E, F, H, J, P, N, K, are CPU Address Outputs A0 thru A12 respectively, to the cartridge. The CPU can address an 8K byte segment of memory resident in the cartridge using these lines.

PINS 10, 9, 8, L, 6, 7, 11, M are the CPU data lines (D1) thru D7 respectively.

PIN 13 is the Vcc pin with a nominal voltage of 5Vdc.

PIN 8 is the GROUND reference to the cartridge.

#### ELECTRICAL LEVELS:

The Address Outputs (A0 thru A12), the Data Lines (D1) thru D7) during a CPU write cycle, the R/W output and the B02 Output have the following drive capability:

HIGH STATE:  $V=2.7$  Vdc (min):  $I=20$  microamps (min source current)

LOW STATE:  $V=0.5$  Vdc (max):  $I=8$  mA (max sink current).

The CCNTL output, and the select lines, S4 and S5, have the following drive capability:

HIGH STATE:  $V=2.7$  Vdc (min):  $I = 400$  microamps (min source current)

LOW STATE:  $V= 0.5$  Vdc (max):  $I=8$  mA (max sink current)

The RD4 and RD5 inputs shall source a minimum of 7mA at 3Vdc.

The data lines (D0 thru D7) during a CPU read cycle should have the following drive capability:

HIGH STATE:  $V=2.4$  Vdc (min) at 220 microamps (minimum source current)

LOW STATE:  $V=0.4$  Vdc (max) at 3.2 milliamps (minimum sink current)

	<u>S4</u>	1	A	RD4	
	A3	2	B	GND	
	A2	3	C	A4	
	A1	4	D	A5	
	A0	5	E	A6	
	D4	6	F	A7	
	D5	7	H	A8	
	D2	8	J	A9	
	D1	9	K	A12	
CONSOLE	D0	10	L	D3	CONSOLE
BOTTOM	D6	11	M	D7	TOP
	<u>S5</u>	12	N	A11	
	+5V	13	P	A10	
	RD5	14	R	R/W	
	<u>CCNTL</u> (Y5)	15	S	B02 (was RAS)	

*opposite polarity,  
narrower*

FIGURE 5.3 CARTRIDGE INTERFACE  
 (LOOKING INTO THE CARTRIDGE SLOT)

### 5.1.1.3 MONITOR INTERFACE

The monitor interface is a 5 pin DIN connector (see figure 5.4) with the following pin-out:

PIN 1 is the real time Composite luminance output. This signal has a voltage level between 0 and 1 volt AC. This output has an impedance of 75 ohms (looking into the pin). This output contains the luminance and sync information. It does not contain the chrominance information.

PIN 2 is the GROUND reference signal to the monitor.

PIN 3 is the real time monoaural audio output to the monitor. This signal has a peak-to-peak variation of 1 volt. This output has an impedance of 1.8K ohms (looking into the pin). *has the clipping problem been addressed?*

PIN 4 is the real time Composite Video output to the monitor. This signal has a variation between 0 and 1 volt. This output has an impedance of 75 ohms (looking into the pin). This output contains the luminance, chrominance and sync information.

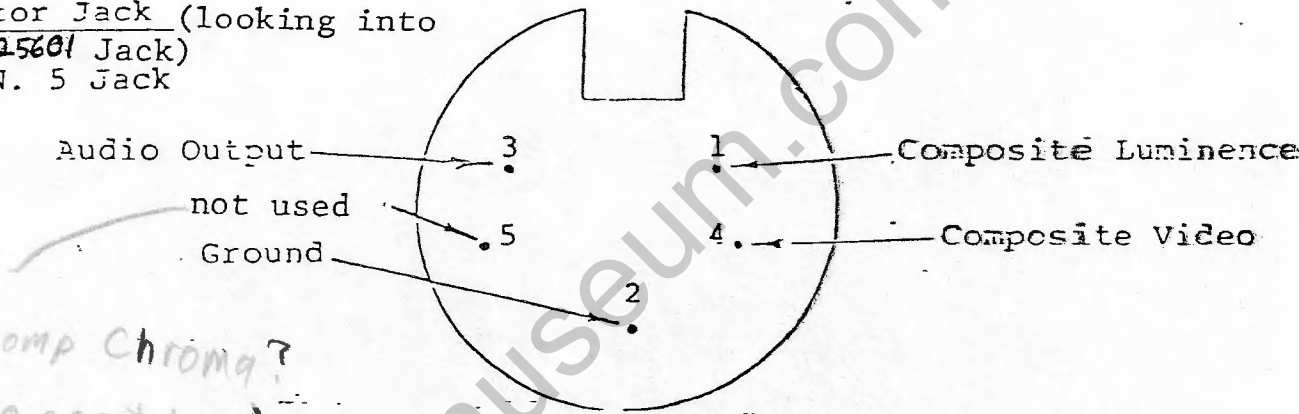
PIN 5 is the no connect.

### ELECTRICAL LEVELS

The composite luminance and composite video characteristics with a 75 ohm termination:

SYNC TIP	MAX 0.08V
BLACK LEVEL	0.35 +- 10%
WHITE LEVEL	0.70 +- 15%

Monitor Jack (looking into  
the 25601 Jack)  
D.I.N. 5 Jack



was comp Chroma?  
(no great loss)

Figure  
5.4

NOT RELEASED

5.1.1.4 SIO INTERFACE

The SIO bus is an asynchronous serial bus capable of transmitting data at 19,200 baud. The physical connection to this bus is via a 13 pin connector. See Appendix 1.4 for the software protocol for the SIO interface.

ATARI SIO CONNECTOR PIN ASSIGNMENT

13 Pin Connector

- 1-2 Not Used
- 3 Data In - 19,200 Baud Data Line to the Computer
- 4 Signal Ground
- 5 Data Out - 19,200 Baud Data Line to the Computer
- 6 Signal Ground
- 7 Command/ - from the Computer goes to Zero (low) when a Command Frame is being sent from the Computer
- 8-9 Not Used
- 10 Ready
- 11-13 Not Used

limits max data xfer rate severely

deletion of 8,9,11,13 have sever impact on expandability, performance of subsequent sio peripherals.

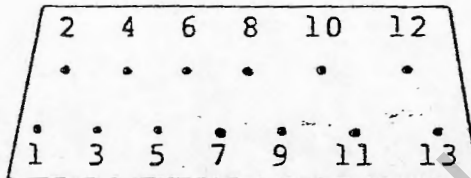
SIO ELECTRICAL SPECIFICATION

PERIPHERAL INPUT	VIH	2.0V DC (MIN)
	VIL	0.4V DC (MAX)
	IIH	20.0 UA DC (MAX) @ 2.0V VIH
	IIL	5.0 UA DC (MIN) @ 0.4V VIL
PERIPHERAL OUTPUT (OPEN COLLECTOR)	VOL	0.4V DC (MAX) @ 1.6 MA
	VOH	4.5V DC (MIN) @ 100K OHM R(EXT)
READY/VCC (5V)	VIH	2.0V DC (MIN) @ 1.0 MA IIH
	VIL	0.4V DC (MAX)
	VIL	0.0V DC WHEN DISCONNECTED

AUDIO INPUT

100 mV (peak to peak) audio signal  
Input impedance 1000 Ohms.

why spec a non-existent pin



- |                 |                   |
|-----------------|-------------------|
| 1. Clock Input  | 8. Motor Control  |
| 2. Clock Output | 9. Proceed        |
| 3. Data Input   | 10. +5/Ready      |
| 4. Ground       | 11. Audio Input   |
| 5. Data Output  | 12. Not Connected |
| 6. Ground       | 13. Interrupt     |
| 7. Command      |                   |
- they're back 171*

25601 SIO CONNECTOR  
 (looking into the 25601 Jack)

NOTE: See SIO Users Manual  
 Part 1 for a description  
 of the signals.

5.1.1.5 TV INTERFACE

An integrated RF modulator (see reference [14]) will be supplied to provide the signals to interface to a standard NTSC television. The RF modulator will have the following characteristics with a 75 ohm termination at its connector:

Maximum voltage: 2 mV  
Minimum voltage: 1 mV

The Modulator output is selectable via a switch to channel 2 or channel 3.

	<u>BAND</u>	<u>PICTURE CARRIER</u>	<u>SOUND CARRIER</u>
CHANNEL 2	54-60 MHz	55.25 MHz	59.75 MHz
CHANNEL 3	60-66MHz	61.25 MHz	65.75 MHz



### 5.1.2 8088 I/O

All functions represented in the block diagram (Fig. 4.1) for the 8088 will be implemented. The intent is to maintain complete hardware compatibility with the IBM type of personal computer.

#### 5.1.2.1 KEYBOARD


The 25601 keyboard will represent as closely as possible the mechanical (keyboard layout and connector compatibility) and electrical (keycodes) as the keyboard represented in the Technical Reference Manual pages 1-31, 1-32, & 1-33. (See [10]).

The keyboard interface shall be such that the 25601, when running Atari XL home computer family compatible programs, will emulate the current Atari keyboard. This means that it will have the capability of supporting the OPTION, SELECT, and START keys of the Atari keyboard. The RESET key will be located on the main control unit rather than the keyboard. The other Atari specific keys must be located on the keyboard. The keyboard will have a mechanism for adjusting the keyboard height. See Appendix 1.5 for more detail.

The keyboard layout is shown in Figure 5.5. The keyboard connector pin definition is shown in Figure 5.6.

The size of most of the keys on the keyboard will be identical to that on the IBM Personal Computer. All of the keys will have full size tops, instead of the smaller tops as on some of the IBM Personal Computer keys (see Appendix 1.5 for details). The tactile feel of the keyboard will be at least as good as the Atari 1200XL computer keyboard. The keyboard layout and labeling must be identical to that of the IBM keyboard, with the following exceptions:

3 Additional Keys 'START', 'SELECT', and 'OPTION' mounted on the right edge of the keyboard (see Appendix 1.5 for suggested placement of these keys)

Keytop of F10 key also bears the legend used on the Atari 1200 family of home computers to indicate the reverse video key, '  '.

The keytop of the return key also bears the legend 'RETURN' below the arrow

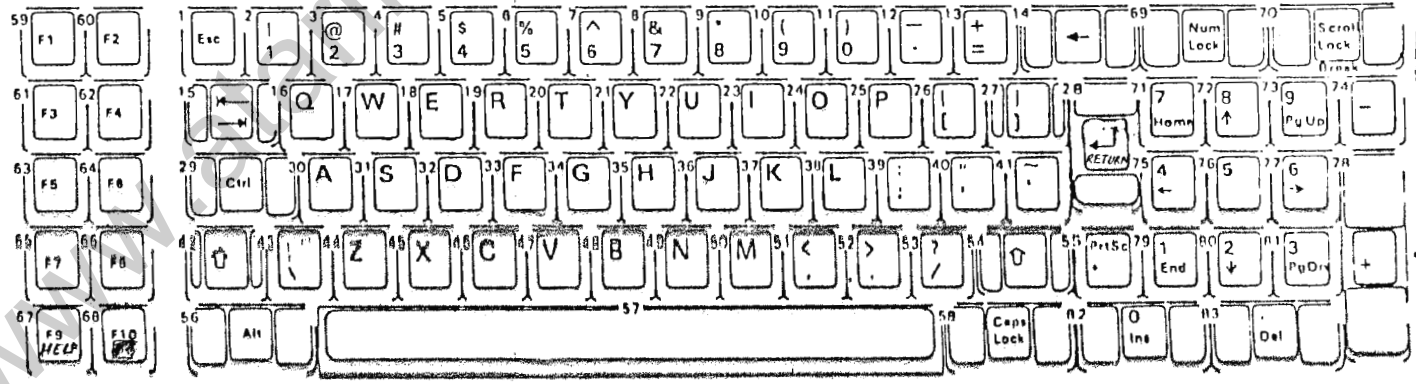
#### OPERATING LIFE

Ten million operations each key.

NOT RELEASED

Fig. 5.5

Keyboard Diagram



Note: Nomenclature is on both the top and front face of the keybutton as shown. The number to the upper left designates the button position.

PIN #	FUNCTION
1	+ KEYBOARD CLK
2	+ KEYBOARD DATA
3	- KEYBOARD RESET (NOT USED BY KYBD)
4	GROUND
5	+5 VOLTS
6	'START'
7	'SELECT'
8	'OPTION'

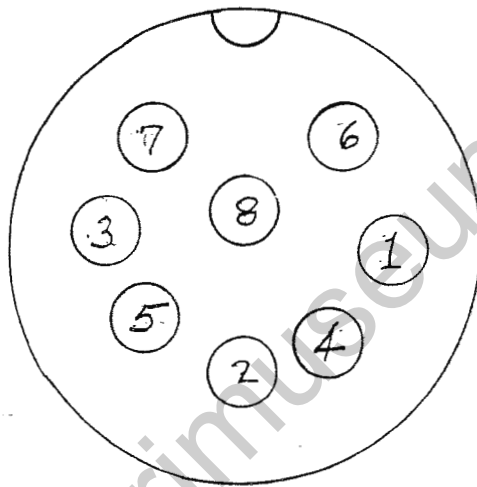


Figure 5.6  
 Keyboard Connector  
 (LOOKING INTO THE 25601 CONNECTOR)

NOT RELEASED

Keys must operate freely without drag, squeaking, or abnormal noise under normal operating conditions.

boils down to  
20grams key-~~key~~  
50 grams kbd-~~key~~

The average key actuation force must be 60 grams +/- 25 grams. Actuation force of each key on a given keyboard assembly must be within 10 grams of the average actuation force of that keyboard. The space bar should withstand 200 free-falls of 3 pounds from a 3/4 inch height.

#### 5.1.2.2 EXPANSION SLOTS

The 25601 shall provide four user accessible expansion slots internal to the machine, capable of accepting and running IBM personal computer compatible expansion cards. The electrical requirements of these card slots are described in the Technical Reference Manual pages 1-15 to 1-19 (see [10]).

#### 5.1.2.3 SPEAKER

The 25601 will have an internal speaker capable of supporting IBM PC and Atari programs. See page 1-20 of the Technical Reference Manual (see [10]).

#### 5.1.2.4 DISK I/O

The 25601 will be capable of supporting a maximum of two integral 5-1/4" disk drives. These disk drives, with their support circuitry, will be capable of reading and writing diskettes that are compatible with diskettes on the IBM personal computer. These disk drives will also be capable of reading and writing diskettes that are compatible with the Atari 1050 disk drive. This means that in the Atari mode, the disk controller must be capable of reading and writing both soft and hard sectored media.

One double-sided disk drive will be offered in the standard 25601 configuration. This standard drive will be mounted in the left-most drive position. A second drive may optionally be installed in the cabinet. The machine will provide all firmware and hardware necessary to support this second drive. This includes a power source for the second drive. The 25601 will be designed so that the second drive is user installable.

#### 5.1.2.5 CONFIGURATION SWITCHES

The 25601 will have two 8 position DIP switches similar to those on the IBM personal computer. (See Technical Reference Manual pages 1-13 & 1-14, referenced in [10].) These switches will also be located at the same addresses as those on the IBM computer, to facilitate maximum

compatibility.

[www.atarimuseum.com](http://www.atarimuseum.com)

5.1.3 POWER SUPPLY SPECIFICATIONS

The Atari 25601 power supply will meet the following requirements:

Input Voltage:	120 VAC +/- 10% @ 60 Hz. +/- 1 Hz.
Power Cord and Plug:	detachable 8 foot U.S.A. 3 prong type, must meet UL/CSA standards
Power Switch:	rocker type
Power-on Indicator:	red LED visible on the keyboard, illuminated when +5 VDC is active

The 25601 will also have a fuse. The specifications of the fuse are dependent on the power requirements and are to be specified. The fuse should be user replacable without exposure to dangerous voltages. The fuse may be housed within the power supply unit similar to the IBM-PC.

## 5.2 MECHANICAL REQUIREMENTS

### 5.2.1 APPEARANCE

The photograph in Figure 5.6 shows a suggested implementation of the Atari 25601 industrial design. The suggested line drawings for this implementation can be found in Appendix 1.5, along with details on the suggested coloring, texturing, and material usage scheme for the machine. *not included*

The 25601 shall have a detachable full-stroke keyboard with layout as detailed in Section 5.1.2.1. The keyboard shall connect to the main unit with a coiled cable. The cable shall have an 8-pin male DIN connector at the main unit end. There will be no connector at the keyboard end of the cable. The cable shall have a length of 2 feet when coiled, and approximately 4.5 feet when fully extended.

The main unit shall have dimensions similar to the IBM PC. Suggested dimensions are shown in Appendix 1.5. The main unit shall be designed so that a user can easily install expansion cards in the internal slots. The machine shall be designed so that all IBM PC compatible expansion cards function when installed. The machine will thus provide card connector openings for each slot and card slot guides. The size of these openings and their position relative to the card edge connector shall be identical to that in the IBM PC.

The main unit housing shall be designed to support a monitor or a television weighing up to 40 pounds (approximately 19 kilograms) on top of the cabinet, - with

*no adverse effects on ventilation (heat)*

Suggested Implementation of Industrial Design

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Figure 5.6



## 5.2.2 DIMENSIONAL REQUIREMENTS

### 5.2.1.1 CONTROLLER JACK

The controller jacks on the 25601 will be 9 pin sub-miniature 'D' type connectors. They will be equivalent to Atari #CO 10448. See Fig. 5.7.

### 5.2.2.2 CARTRIDGE SLOT

The cartridge slot shall be designed to accept a standard Atari cartridge, whose dimensions are shown in Fig. 5.8. The connector for the cartridge is a 30 position edge connector (see Fig. 5.9a). The connector is electrically connected as indicated in section 5.1.1.2. Fig. 5.9b shows the mechanical requirements for the Atari cartridge guide. The cartridge slot should be designed so that the 25601 with the cartridge plugged-in meets all FCC requirements of section 6.0.

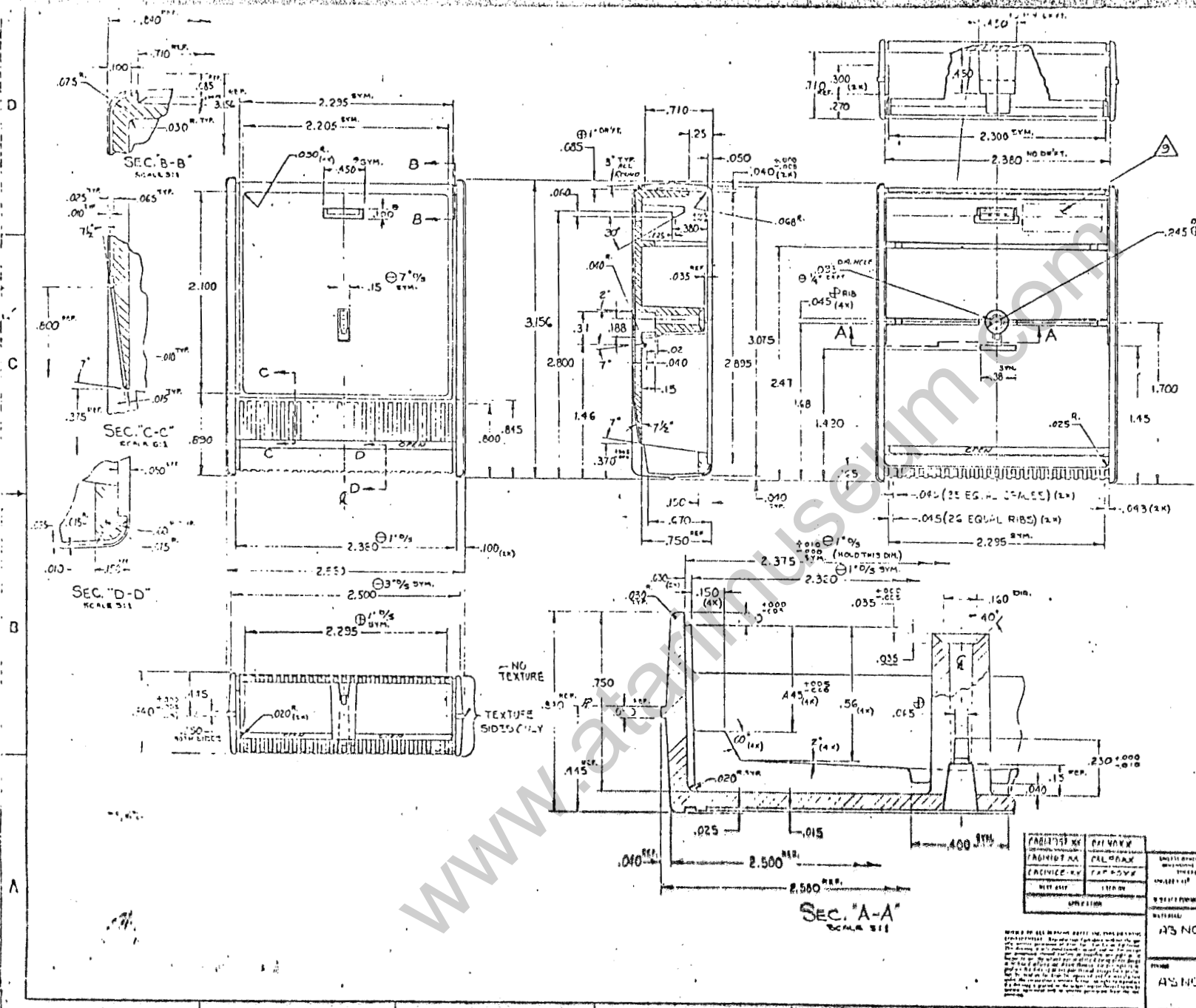
### 5.2.2.3 MONITOR CONNECTOR

The connector for the monitor interface (see section 5.1.2.3) is a 5 pin DIN connector. This connector shall be equivalent to Atari #CO 14388 (see Fig. 5.8).

### 5.2.2.4 SIO INTERFACE

The SIO connector shall be equivalent to Atari #CO 12995 (see Fig. 5.9). This connector is a 13 pin connector and mates to an Atari I/O cable #CAO 14122 (see Fig. 5.10).





1	157-100-0000-0000	157-100-0000-0000
2	CHECKED BY: [Signature]	157-100-0000-0000
3	DRAWN BY: [Signature]	157-100-0000-0000
4	REVISED BY: [Signature]	157-100-0000-0000
5	PRODUCTION RELEASE	157-100-0000-0000
6	REV. PER: [Signature]	157-100-0000-0000
	A-3 DELETED	
	A-3 ADD	

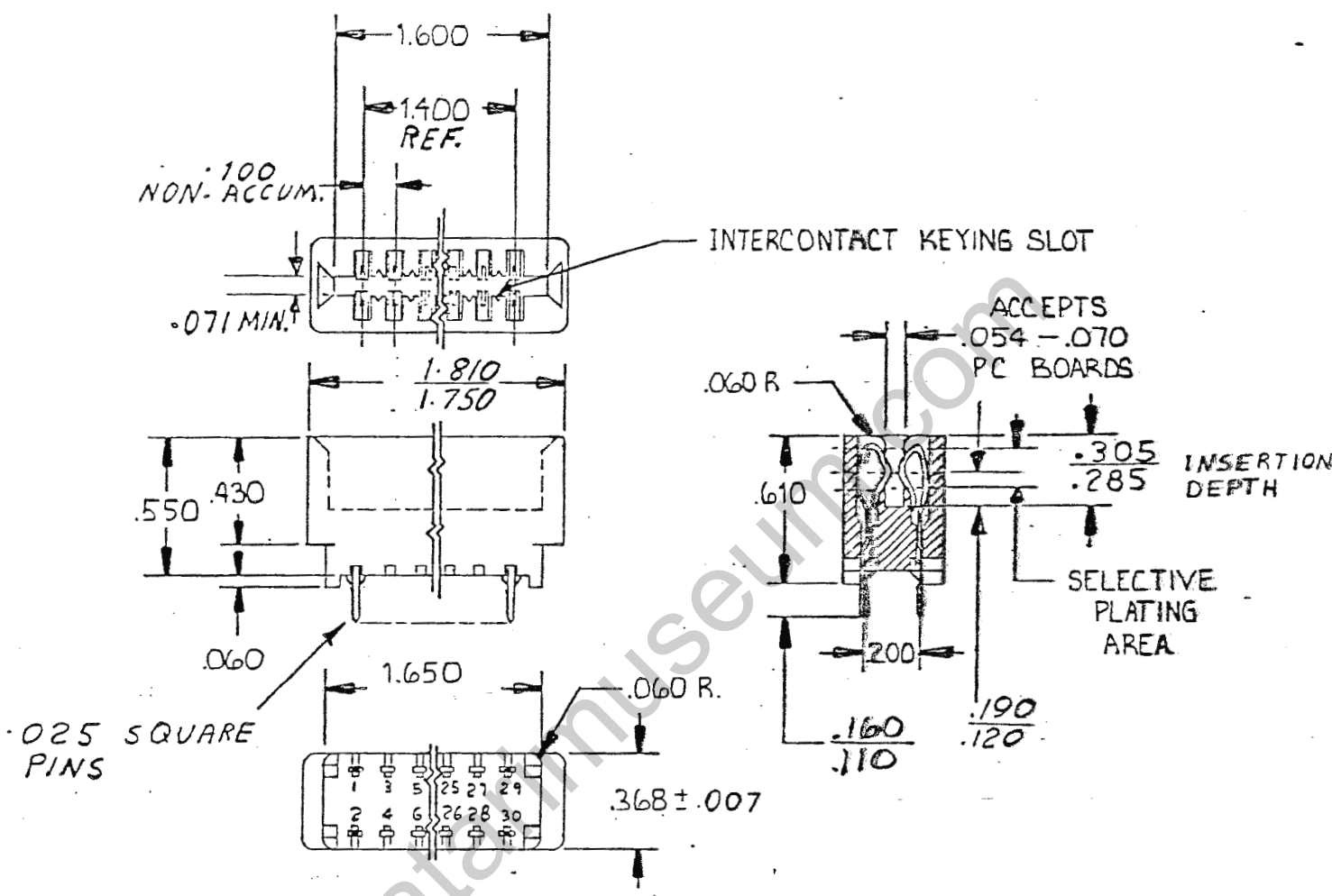
FIGURE 5.8

11. PART TO BE FREE OF DEFECTS AND REWORKED FOR REWORK DEFECTS.
12. ALL DIMENSIONS UNLESS OTHERWISE SPECIFIED.
13. HOLE DIMENSIONS UNLESS OTHERWISE SPECIFIED.
14. FINISH LINE PLACES FOR MAX.
15. GATE REMOVABLE (NO MAX), REWORKED FOR MAX.
16. GATE SUBJECT TO REWORK FOR DEFECTS BY ATARI ENGINEER.
17. WALL THICKNESS: .002 IN. (MAX.)
18. TEXTURE: MT-1013 (4X) (1/4") LOC. ON BOTH SIDES.
19. COLOR: (DK. BROWN) CYCLOAC 132553
20. MATERIAL: .002" TYP. ALL DIMENSIONS APPLY TO THIS DRAWING.
21. DRIFT ANGLE: 1/2" (Ø) PLUS DRIFT/Ø - MINIMUM

NOTES: UNLESS OTHERWISE SPECIFIED

CHECKED BY: [Signature] DRAWN BY: [Signature] REVISED BY: [Signature] DATE: [Date]	DATE: [Date] TIME: [Time]	DO NOT SCALE DRAWING [Signature] [Signature]	ATARI (804) CARTRIDGE HOUSING PART NO. CO12958
MATERIAL: AS NOTED FINISH: AS NOTED	[Signature] [Signature]	[Signature] [Signature]	[Signature] [Signature]

REV	REVISIONS DESCRIPTION	DATE	APPROV



15 DUAL POSITIONS

FIGURE  
5.9a  
OUTLINE AND DIMENSIONS

NOTE: UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE IN INCHES WITH ± .005 TOLERANCE

**NOT RELEASED**



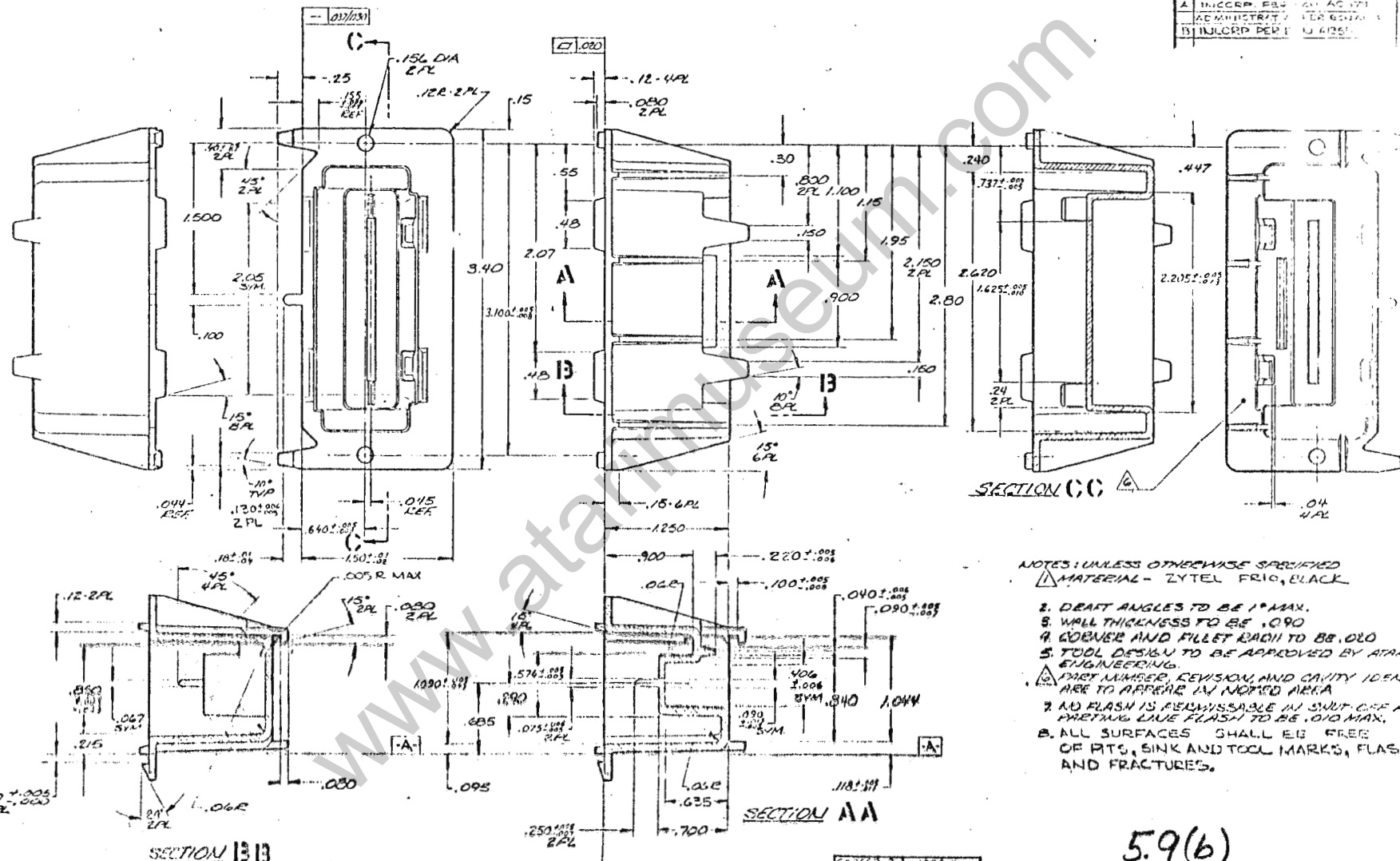
Atari, Inc.  
30 E. Plumaria Drive  
San Jose, CA 95134

A Warner Communications Company

SIZE <b>A</b>	DRAWING NO. CO14389	REV <b>C</b>
SCALE	SHEET 4 OF 4	

8 7 6 5 4 3 2 1

REV	DESCRIPTION	DATE
A	INCCORP. REV. 20 AC 171	
B	ADMINISTRATIVE PER GENVA	
C	INCCORP. REV. 10 4385	



- NOTES: UNLESS OTHERWISE SPECIFIED  
 ▲ MATERIAL - ZYTEL FRIG, BLACK
- DEAST ANGLES TO BE 1° MAX.
  - WALL THICKNESS TO BE .090
  - CORNER AND FILLET RADIUS TO BE .020
  - TOOL DESIGN TO BE APPROVED BY ATARI ENGINEERING
  - PART NUMBER, REVISION, AND CAVITY IDENT. ARE TO APPEAR IN NOTED AREA
  - NO FLASH IS PERMISSIBLE IN SPLIT OFF AREAS. PARTING LINE FLASH TO BE .010 MAX.
  - ALL SURFACES SHALL BE FREE OF PITS, SINK AND TOOL MARKS, FLASH AND FRACTURES.

5.9(b)

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CA06C207	1200XL	APPROVED BY	DATE
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TOLERANCES UNLESS OTHERWISE SPECIFIED		DATE	
ANGLES ± 1°		DATE	
HOLE POSITION ± .010		DATE	
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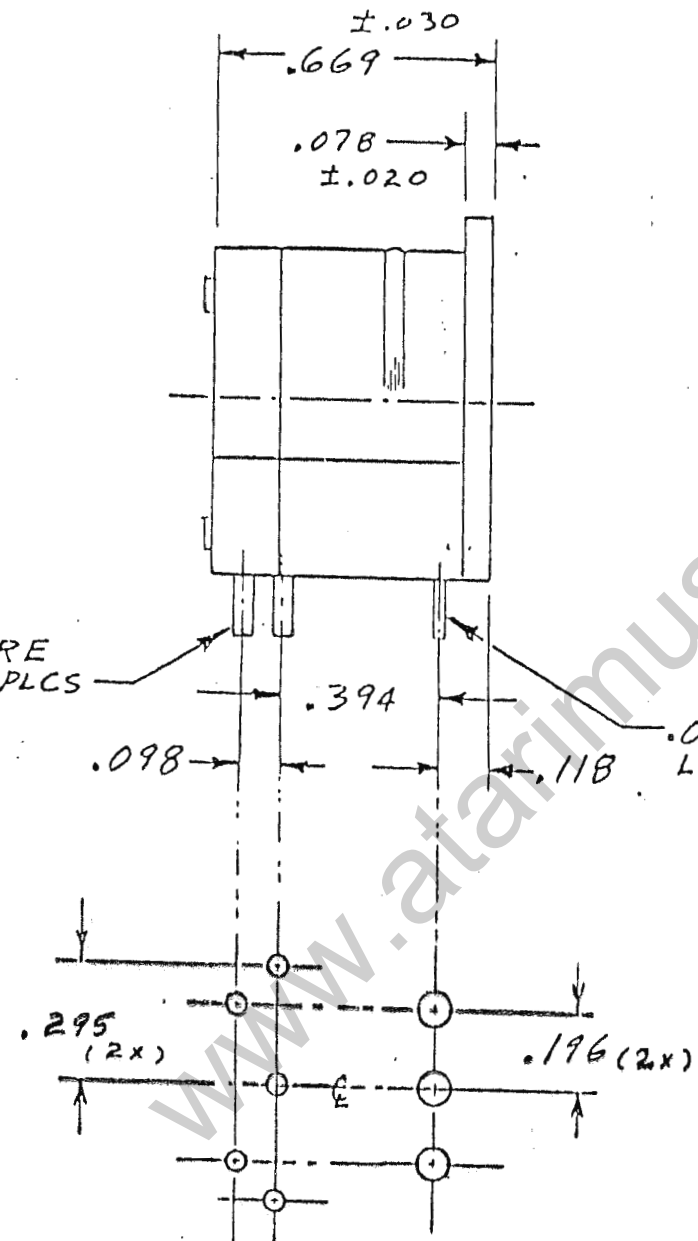
SIZE A  
DRAWING NO. C014388

SCALE 2 X  
SHEET 4 OF 4

REV B

NOT RELEASED

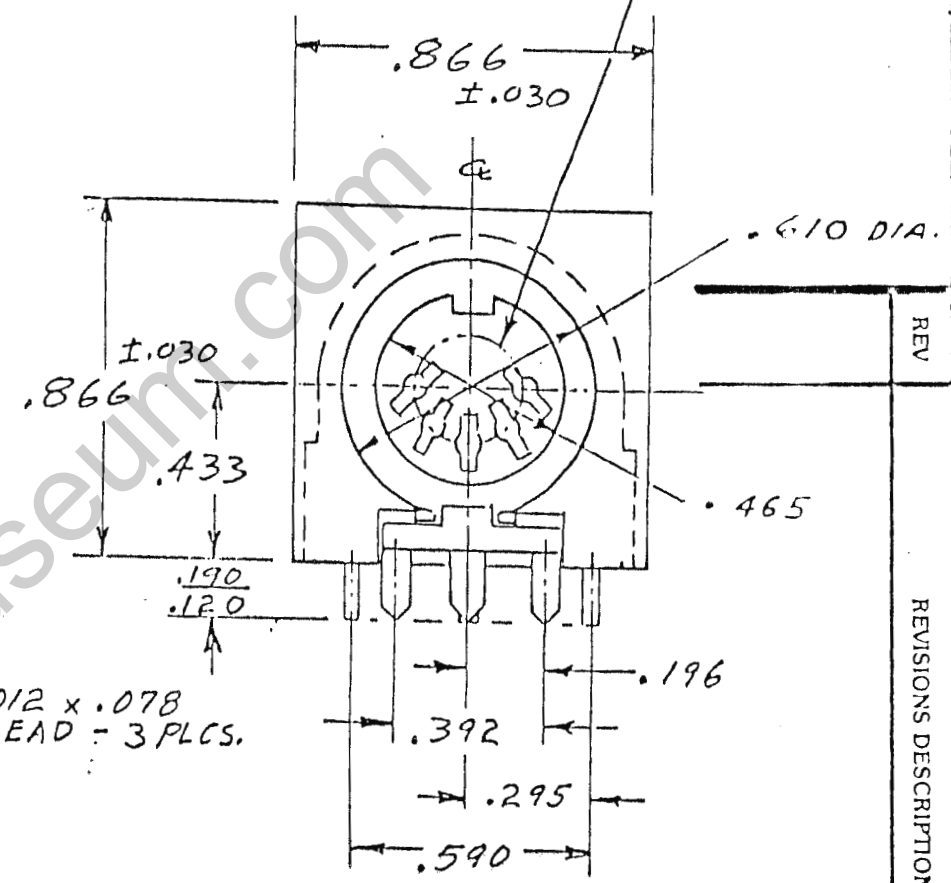
.031 SQUARE LEAD - 5 PLCS



.012 x .078 LEAD - 3 PLCS.

PCB MOUNTING DETAIL

5 RECEPTACLES ON .275 DIA. B.C.



DIMENSIONS ARE IN INCHES,

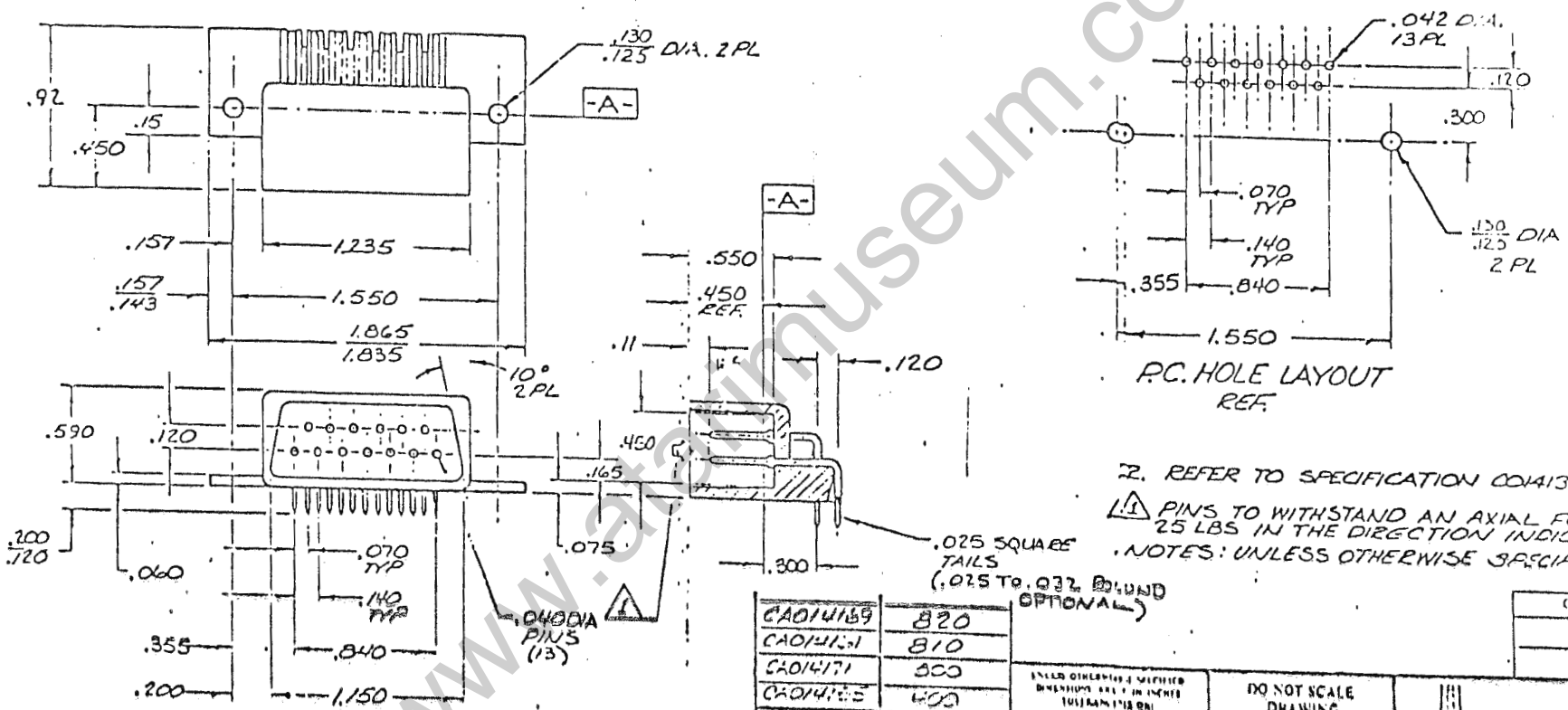
TOLERANCE :  $\pm .005$

FIGURE 5.10 UNLESS OTHERWISE

REV	REVISIONS DESCRIPTION	DATE	APPRO

NOT RELEASSED

4	REDRAWN & REVISED	1/10/79
A	PRODUCTION RELEASE	1/10/79
B	REVISED PER ECN # 10346	1/10/79
C	REVISED PER ECN # 10158	1/10/79
D	REV PER ECN # 10357	1/10/79



2. REFER TO SPECIFICATION COA132.  
 ⚠ PINS TO WITHSTAND AN AXIAL FORCE OF 25 LBS IN THE DIRECTION INDICATED.  
 NOTES: UNLESS OTHERWISE SPECIFIED

CA014169	820
CA014171	810
CA014171	800
CA014175	400

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES (US STANDARD)	DO NOT SCALE DRAWING
SCALE: 1" = 1.00"	DATE: 23 FEB 79
DESIGNED BY: [Signature]	DATE: 23 FEB 79

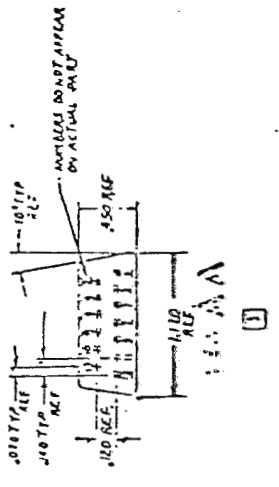
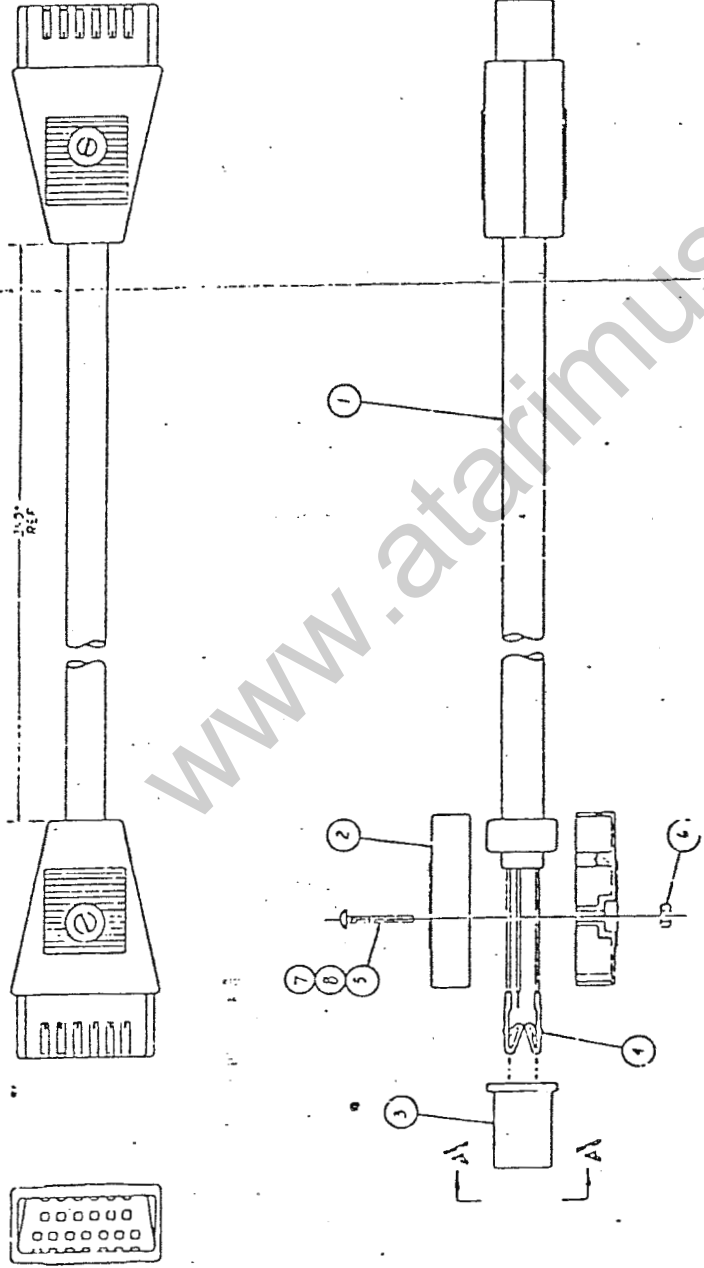
OUTSTANDING ECNs	
ATARI, Inc. 1265 Bellevue Avenue Sunnyvale, Calif. 94085	
ATARI	

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MATERIAL: ADAPTER - A. J. MON (BLACK)  
 PINS - BRASS  
 FINISH: PINS - 15:24 IN TIN OVER 304 IN NICKEL

TITLE: CONNECTOR 13 PIN - RIGHT ANGLE	
DATE: 2/20/79	DRWING NO: C012995
SCALE: 2/20/79	REV: 0

FIGURE 5.11



CONDUCTOR	COLOR CODE
1	BROWN
2	RED
3	ORANGE
4	PINK
5	YELLOW
6	GREEN
7	BLACK
8	WHITE
9	BLUE
10	WHITE/BLACK
11	BLACK
12	GRAY

ITEM NO.	DESCRIPTION	QTY
1	1/10 CABLE SUBSTRATE	1
2	1/10 CABLE SHIELD	1
3	1/10 CABLE JACKET	1
4	1/10 CABLE INSULATION	1
5	1/10 CABLE Braid	1
6	1/10 CABLE SOLDER	1
7	1/10 CABLE NUT	1
8	1/10 CABLE SCREW	1

ITEM NO.	DESCRIPTION	QTY
1	1/10 CABLE ASSEMBLY	1
2	1/10 CABLE SUBSTRATE	1
3	1/10 CABLE SHIELD	1
4	1/10 CABLE JACKET	1
5	1/10 CABLE INSULATION	1
6	1/10 CABLE Braid	1
7	1/10 CABLE SOLDER	1
8	1/10 CABLE NUT	1
9	1/10 CABLE SCREW	1

1. TUBULAR RIVETS OR EYELETS MUST BE USED IN PLACE OF MACHINE SCREWS AND NUTS.
2. ASSEMBLY OPERATOR SHALL LEAVE 1/16" TO 1/8" SPACE BETWEEN AND SHALL INSURE WITH TIGHT PART NO. CORRECT.
3. COMPLETED CABLE SHALL BE TESTED FOR CONTINUITY WITH TESTER. SHOULD BE SOME SINGLE PLUGGED INTO A RINGING CONNECTION. THERE SHALL BE NO INTERMITTENT SIGNALS.
4. CONDUCTOR INSULATION SHALL BE INSPECTED FOR ANY CRACKS, DISINTEGRATION AND DISCOLORATION. IF ANY OF THESE DEFECTS ARE FOUND, THE CABLE SHALL BE REJECTED.

NOTE: THESE DIMENSIONS ARE APPROXIMATE

ATARI 0	1/10 CABLE ASSEMBLY
D	CA014122

FIGURE 5.12

NOT RELEASED



### 5.3 Software Requirements

This section describes the hardware features necessary to support the desired software for the Atari 25601. The details of the software specification are described in a separate document (25601 Software External Reference Specification).

There will be a total of 16K of ROM and 64K of RAM on the 8088 sub-system. The Shakti main circuit board will also contain sockets for the addition of another 64K of RAM for the 8088 sub-system. The SALLY sub-system will include 28K of ROM and 64K of RAM. The 28K of ROM will be logically organized as a 16K operating system ROM, an 8K Atari BASIC interpreter, and two independent device handler ROMs of 2K each. Each of the device handler ROMs can be individually bank selected into the D800-DFFF region. All of the system ROMs will be mounted in sockets.

#### 5.3.1 Dual Processor Software

~~Both~~ The 8088 and SALLY shall be able to run simultaneously. Each will be able to generate a maskable interrupt for the other processor. In addition, the inter-processor communications hardware will be capable of generating DMA requests within the 8088 sub-system.

When either processor is executing a task, the other processor may be used as an auxiliary processor or as an I/O processor. One example of this use is when running Atari software on the SALLY sub-system. The 8088 processor will be responsible for reading the key-depressed/key-released codes from the keyboard and translating them to the appropriate Atari keyboard matrix codes. These keyboard codes will be written into a hardware interface which is writable from the 8088 I/O address space, and which emulates the keyboard matrix expected by POKEY in the SALLY sub-system.

The panel mounted RESET switch shall reset both processors.

### 5.3.2 SALLY Software

Ideally, all Atari XL family applications software that does not use the integral modem will be able to run without modification on the Atari 25601, provided that they were written using good programming practices. Good programming practices include the use of proper operating system entry points, entry conditions, and public operating system database elements. *This eliminates much (if not most) Atari software*

All registers in the SALLY address space for the peripheral chips (ANTIC, POKEY, GTIA, PIA, etc.) will be at the same addresses and have the same definitions as in the Atari 1200XL family of home computers. The additional registers are detailed in Figures 5.13b1, 5.13b2, and Appendix 1.3.

#### 5.3.2.1 SALLY Operating System

The operating system for the SALLY sub-system will occupy 16K of ROM space. The Atari BASIC interpreter will occupy another 8K of ROM space. An additional 4K ROM will be provided that will contain two independent device handlers of 2K each. Each of these logical ROM spaces may be disabled under software control to provide access to the underlying RAM. Additionally, the 2K region of the operating system ROM that would normally occupy the same address region as the Atari 25601 I/O addresses can be mapped to low memory under software control (see Figure 5.13a).

The Atari 25601 will provide the same speech software functionality as the speech device available in the Atari 1200 family of computers. Internally, the software will differ to accommodate the fact that the speech chip and its support circuitry are directly within the SALLY address space rather than appearing as a PBI (Parallel Bus Interface) device. 2K of bank-selected ROM which can be made to overlay the MATHPAK area is available for this function. *either no speech or no math or no SIO for 8088*

#### 5.3.2.2 SALLY Peripheral Support for 8088 Sub-system

The Atari 25601 software will permit programs running on the 8088 processor to use the SIO printers and serial interfaces. A 2K handler ROM is available to provide Inter-Processor Communications support.

#### 5.3.2.3 SALLY Memory Map

The Atari 25601 memory map for the SALLY processor is detailed in Figures 5.13a and 5.13b. The SALLY can select alternate ROM code to overlay the MATHPAK area (D800-DFFFH) by writing to a register in the PIA. There will be two logically separate device handler ROMs of 2K each that can be made to occupy this region in place of the normally selected operating system ROM.

### 5.3.3 8088 Software

The 25601 will contain 16K of ROM in the address space of the 8088 sub-system, beginning at address OFC000H. This ROM will include both the Basic Input Output System (BIOS) and Inter-Processor Communication support.

#### 5.3.3.1 Operating System

The Basic Input Output System (BIOS) for the 8088 processor will be resident in ROM. The BIOS will use a set of interrupt service entry points compatible with the IBM PC (see Technical Reference [10]). The BIOS will also be extensible by a means compatible with the IBM method of having ROM resident on peripheral cards. The functions of the BIOS may also be supplemented or replaced by code read from disk or cartridge.

The Atari 25601 will support Microsoft's MS-DOS Versions 2.0 and 1.25. There shall be no hardware restrictions to prevent future upgrades to Digital Research CP/M-86, Concurrent CP/M-86, or the UCSD p-SYSTEM.

#### 5.3.3.2 Peripheral Support for SALLY System

While the SALLY sub-system is running programs such as those designed for the Atari 1200 family of home computer systems, the 8088 sub-system is available to provide I/O functions within the 25601 system. The 8088 will provide access to Atari 1050 formatted diskettes which can be read and written when inserted in the integral disk drive(s). The 8088 sub-system is also responsible for receiving information from the intelligent keyboard and converting it into a form usable by the hardware emulation of the POKEY keyboard matrix.

#### 5.3.3.3 8088 Memory Map

The memory map, I/O space, and interrupt allocations for the 8088 sub-system of the 25601 are illustrated in Figures 5.13c, 5.13d, and 5.13e respectively.

SALLY Memory Map for 25601

FFFF	Operating system if ROM ENABLE asserted;
E000	RAM if ROM ENABLE not asserted.
DFFF	if ROM ENABLE asserted then Operating system (MATHPAK), unless a Device Handler ROM is selected by PIA Port B
D800	RAM if ROM ENABLE not asserted.
D7FF	Memory mapped I/O space (see Figure 5.3b for details);
D000	Self Test (Physical) Code Space shadowed by I/O devices
CFFF	Operating system if ROM ENABLE asserted;
C000	RAM if ROM ENABLE not asserted.
BFFF	Mapped to cartridge interface if RD5 asserted;
A000	RAM or Atari BASIC if RD5 not asserted.
9FFF	Mapped to cartridge interface if RD4 asserted;
8000	RAM if RD4 not asserted.
7FFF	RAM
5800	
57FF	Self Test (Logical) Space if MAP enabled and ROM ENABLE asserted;
5000	RAM if MAP disabled or ROM ENABLE not asserted.
4FFF	RAM
0000	

Figure 5.13a

SALLY Memory Mapped I/O Space

D7FF	
D700	RAM (reserved for OS scratchpad)
D600	RAM (reserved for OS scratchpad)
D500	Cartridge Control
D400	ANTIC
D300	PIA
D200	POKEY
D100	Inter-Processor Communication and Speech
D000	GTIA

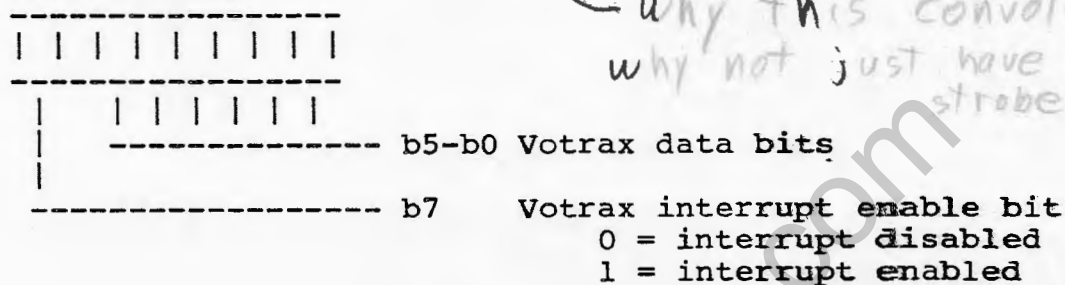
Figure 5.13b1

Additional 25601 SALLY I/O Registers

D100H      Votrax Speech Synthesizer Strobe

Writing don't care data to this register causes the Votrax SC-01 to speak the phoneme previously stored in D110H.

D110H      Votrax SC-01 Speech Synthesizer Control Register  
 (write only)



D301H      PIA Data Port B

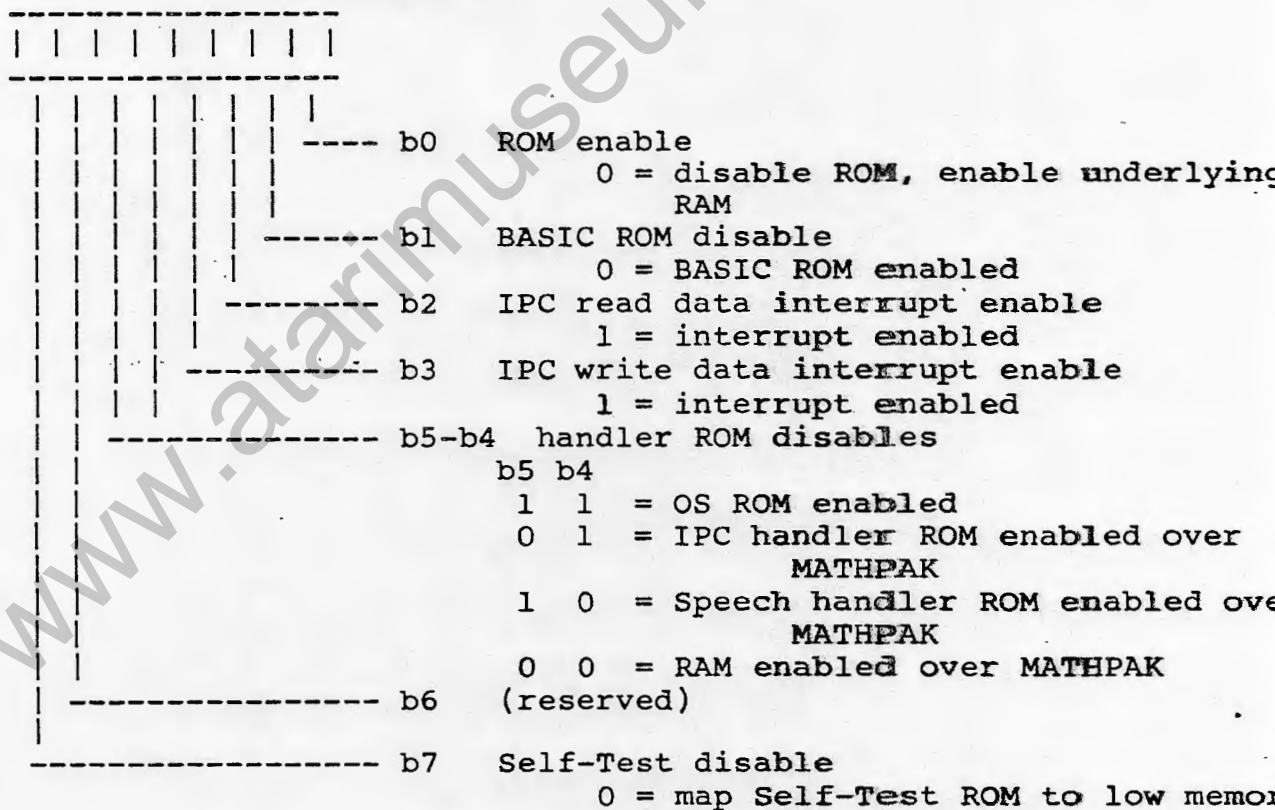


Figure 5.13b2

8088 MEMORY MAP for 25601

FFFF	
FC000	16K System ROM (includes BIOS)
F0000	Reserved
C0000	Reserved for ROM and Control
A0000	Reserved for Memory Mapped I/O Devices
10000	Available for up to 576K RAM Expansion in I/O Channel Slots
00000	64K RAM on Main 25601 Processor Board

Figure 5.13c

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## 8088 I/O MAP for 25601

3F0-3F7	Diskette
0FX	SALLY Keyboard Emulation (alternate)
0E0-0E7	Reserved
0DX	Inter-Processor Communications (alternate)
0CX	Reserved
0AX	NMI Mask Register
080-083	DMA Page Registers
07X	SALLY Keyboard Emulation (primary)
060-063	PPI 8255A-5
05X	Inter-Processor Communications (primary)
040-043	Timer 8253-5
020-021	Interrupt Controller 8259A
000-00F	DMA Controller 8237A-5

Figure 5.13d



## 8088 Interrupt Allocations for 25601

NMI	Parity (on I/O channel)	
7	Reserved (for printer)	higher than disk?
6	Disk Controller	(another 1132?)
5	Interprocessor Communications (primary)	
4	Reserved	
3	Reserved	
2	Interprocessor Communications (alternate)	
1	Keyboard	
0	Timer	lower than keyboard?

Figure 5.13e

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5.4 PRODUCT PERFORMANCE

5.4.1 Environmental Specifications

The Atari 25601 is required to withstand the following test regimen. Please refer to [13] for complete details on these tests.

1. Thermal Mapping performed at room temperature (25'C), 45'C, and at reduced pressure (520 mm Hg, 45'C)

The surface temperature of sensitive components is measured under normal or exaggerated operating conditions. Vendor's temperature limits must not be exceeded, and hot spots on outside of case must not be in excess of 5'C above ambient.

2. Temperature Range (Operational)

10'C to 40'C (50'F to 104'F) for diskettes  
10'C to 45'C (50'F to 113'F) for electromechanical portion

3. Temperature Range (Storage)

-30'C to 60'C (-22'F to 140'F)

4. Humidity Range (Operational)

15% to 90% relative humidity, non-condensing.

5. Humidity Range (Storage)

10% to 90% relative humidity, if condensation does occur, unit must work after drying, excluding damage to the floppy diskettes from the condensation

6. Temperature/Humidity Cycle

Temperature and humidity levels are varied between upper and lower specified limits as listed in items 2, 3, 4, and 5 above, per schedule set in Procedure 3.2.4.4.1 of reference document [13].

7. Salt Spray (Corrosion)

(applies to keyboard, PCB connectors, IC sockets, and other connectors only)

Components suspended at 35'C for 24 hours in an atmosphere containing atomized 1% neutral salt solution sufficient to provide a collection rate of 0.5 to 1.5 ml per hour. Atari will perform this test.

8. Altitude (Operational)

0 to 3000m (0-9840 ft) approx. 520 mm Hg min. atmospheric pressure.

9. Vibration (Operational)

Products to be uneffected by background of 5 to 100 Hz frequency, 0.3 g acceleration, 0.08 inch max. double amplitude displacement.

10. Sine Vibration

Ten minute dwell at all major resonances. Input level shall be 0.015 inches double amplitude or 1.0 g's depending on equipment used. Two cycles from 5 to 100 to 5H at 0.015 inches double amplitude or 1.0 g's depending on equipment used.

11. Random Vibration

Broadband frequency from 10 to 1000Hz, acceleration power spectral density to be 0.04 g<sup>2</sup>/Hz, 6.3g RMS overall, 15 minutes per axis. Atari will perform this test to verify compliance, vendor should perform an equivalent test.

12. Shock (Impact)

Half sine or sawtooth wave form, 30g, 11 msec, 3 shocks in each direction of each axis (total of 18). Atari will perform this test to verify compliance, vendor should perform an equivalent test.

13. Transportation Vibration

The product will be vibrated at an appropriate frequency in each direction that it could normally be shipped per procedure 3.3.4 of reference document [13]. Atari will perform this test to verify compliance, vendor should perform an equivalent test.

14. Package Drop

Twelve drops; six faces, four edges, two corners. Per schedule listed in Procedure 3.3.5 of reference document [13].

15. Electrostatic Discharge

External surfaces are subjected to at least 6 contacts with a probe at -15KV from a 300 pF capacitor through 500 ohm resistance. Metal circuit connector pins are excluded. No loss of data or damage to unit should result.

16. Acoustic Noise Measurement

Atari 25601 Hardware Technical Specifications  
CONFIDENTIAL

08 July 1983

The acoustic noise level should not exceed 60 db (A scale)  
for the Atari 25601.

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5.4.2 RELIABILITY:

The targeted MTBF for the 25601 is 8000 hours continuous Power-On at 25 degrees C for the CPU System and electronics in the floppy disk sub-system.

The MTBF for the spindle, stepping system and head in the disk drive sub-system will be 1200 hours with 15% duty cycle.

The targeted MTTR for the 25601 is 30 minutes (max.), including disassembly.

DISK SUBSYSTEM RELIABILITY SPECIFICATION:

Disk Drive Error Rate:

Soft Errors: 1 per 100,000,000 bits read  
Hard Errors: 1 per 100,000,000,000 bits read  
Seek Errors: 1 per 1,000,000 seeks

Mechanical Wear:

Media life: 3,000,000 Rev/Trk (min.)  
Head life: 54,000,000 Revs. (min.)

6.0 REGULATORY REQUIREMENTS

6.1 EMISSION

The 25601 shall meet all appropriate requirements of FCC Docket 20780, Part 15, subpart J, for Class B devices.

6.2 FLAMMABILITY:

Flammability (Enclosure Material):

UL 94 HB or Better

Flammability (Printed Circuit Board):

UL 94 V-1 or Better

6.3 COMPONENT TEMPERATURE LIMITS, SPACING AND OTHER SAFETY STANDARDS:

UL 94HB, UL 114 and CSA-C22.2 #154 or Better

The enclosure material and other components must not contain cadmium as part of their formulation or as a plating.

Surface coatings shall not contain lead, cadmium, or other added ingredients which are based on compounds of antimony, arsenic, mercury, selenium, or water-soluble barium.

Sharp edges, points, or other cut or puncture points must be avoided.

All small parts or projections that may be grasped by the thumb and forefinger or the teeth, and any captivated parts that protect the user against an increase of the risk of fire, shock, or casualty hazard, must withstand a direct pull force of 15 pounds for one minute, applied in the most unfavorable direction, without separation or damage to the captivating means.

The product must meet all requirements of this section, and all applicable government standards. If there are points which do not conform to the applicable standards, negotiations will be held between Atari and Toshiba to determine compliance.

7.0 PACKAGING SPECIFICATIONS

7.1 LABELS

Appropriate label must be attached to each unit per Atari packaging engineering specifications. The label includes, but not limited to, information pertaining to:

- \*Atari model designation
- \*Atari patent designation (if applicable)
- \*Atari product serialization
- \*Country of origin
- \*FCC and other regulation agency compliance ID and information
- \*Work week code, lot code and vendor code ID (see figure 7.1)

All products will be marked with FCC sight code, product code, serial number and work week and year as shown below:

SSSPCNNNNNNNNMMYY

-----  
: : : :  
: : : : Year  
: : : : Work Month  
: : : : Serial Numbers  
: : : : Product Code  
: : : : FCC Sight Code

EXAMPLE:

XXXXFF00000001083  
: : : :  
: : : : 1983  
: : : : 10TH MONTH  
: : : : SERIAL NUMBER=0001  
: : : : PRODUCT (TBD)  
: : : : FCC SIGHT CODE (TBD)

Specifics on location and material associated with date codes will be provided in packaging specifications which will be included in the procurement documents.

The Product Code will also be supplied to the Vendor.

FIGURE 7.1

7.2.1 INNER PACKING

The inner packing must protect the system and accessories from 10 drops from 24 inches on any one of six surfaces, three edges radiating from one corner without any internal damage. The inner packing must also protect the system and accessories from vibrations of 30 minutes each, 2 directions 90 degrees apart, 100-300 cycles per minute. Packaging must leave surface 0.06 inches at some time. Again, no internal damage is allowed.

It is recommended that the system and accessories be enclosed in an anti-static bag and be fully encapsulated in EPS foam or similar material. The foam enclosure should be of 2 piece construction, i.e., top and bottom, with minimum wall thickness of 0.75 inch. External dimensions will be determined by Atari packaging engineering.

7.2.2 DISPLAY CARTON

Six sided 24 pt. SBS (White Chipboard) folding carton. Printed in 4 colors plus PMS877 silver, with UV or other abrasion resistant coating. All graphics will be specified by Atari. Dimensional aspects of carton are to be specified by the vendor.

7.2.3 SHRINK WRAP (TBD)

Fully packaged product will be shrink wrapped to prevent damage and pilferage.

7.2.4 SHIPPING CARTON

Two shrink wrapped products are to be placed in a corrugated shipping carton. The weight and type of corrugate as well as the number of products per shipping carton are to be specified by Atari.

7.2.5 PACKAGE CONTENTS

- \* 25601 COMPUTER SYSTEM AND KEYBOARD UNIT AND CABLE
- \* OWNERS MANUAL WITH WARRANTY MATERIAL
- \* AC POWER CABLE
- \* ATARI BASIC REFERENCE CARD (TO BE CONSIGNED BY



ATARI)

- \* RF SWITCH BOX
- \* VIDEO CABLE (RCA TO RCA)  
APPROX. 3 METERS IN LENGTH
- \* ATARI PRODUCT CATALOG (TO BE CONSIGNED BY ATARI)

7.2.6 OWNER'S MANUAL

THE OWNER'S MANUAL SHOULD CONTAIN THE FOLLOWING INFORMATION:

- \* UNPACKING INSTRUCTIONS
- \* HOW TO CONNECT THE 25601 KEYBOARD AND POWER CABLE
- \* POWER UP INSTRUCTIONS AND OPERATION WITH OTHER PERIPHERALS
- \* INSTRUCTIONS FOR USER OPERABLE AND ACCESSIBLE SWITCHES
- \* HOW TO INSERT AND REMOVE DISKETTE
- \* A USER LEVEL TROUBLE SHOOTING SECTION WITH A TABLE WHICH LISTS AND ILLUSTRATES OBSERVABLE MALFUNCTION SYMPTOMS AND SUGGESTED REMEDIES
- \* FACTORY SERVICING INFORMATION AND WARRANTY INFORMATION/RETURN CARD
- \* APPROPRIATE FCC WARNING STATEMENTS OF EMI/RFI EFFECTS

Appendix 1.1

Suggested and Recommended Schematic of the SALLY Sub-System

[www.atarimuseum.com](http://www.atarimuseum.com)

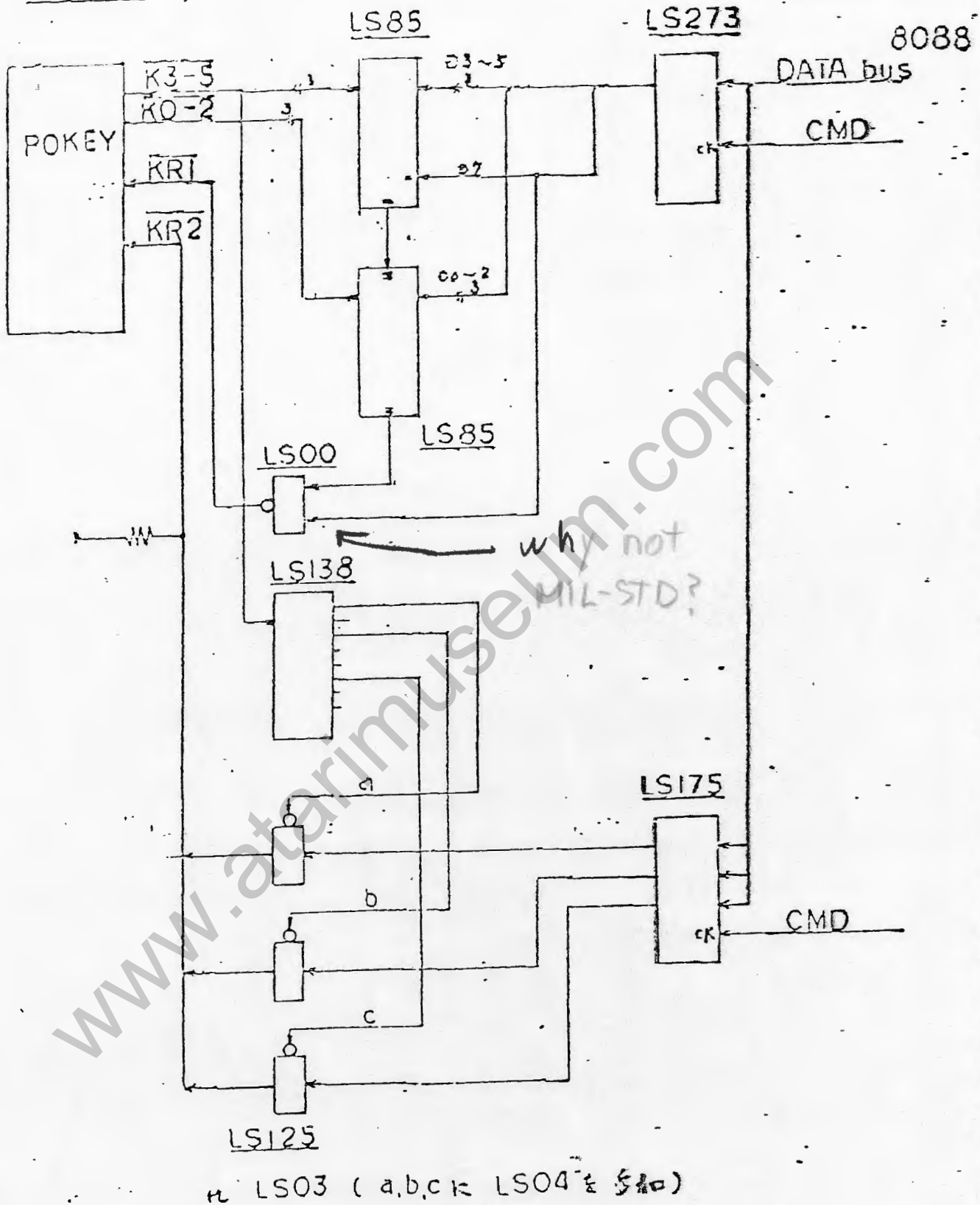
Appendix 1.2

Preferred Keyboard Interface Block Diagram  
for Atari 25601

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6502

8088



LS03 (a,b,c) LS04 & 5th

APPENDIX 1.2

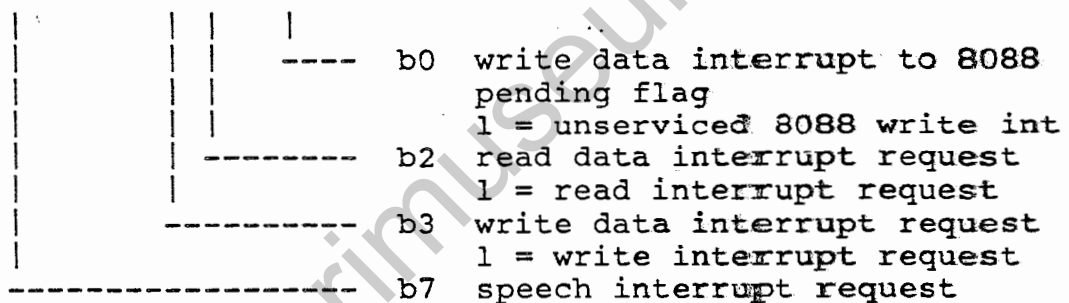
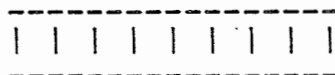
NOT RELEASED

Appendix 1.3

Programmer's Model and Block Diagram  
of the  
Inter-Processor Communication Interface

A1.3.1 SALLY Memory Space

D120H Interrupt Status Register  
(Read only)



D130H-D133H IPC Register Write Register File  
(Write only)

These addresses write to the IPC register file that can be read by the 8088.

Writing any data to D133H causes an interrupt (or DMA) request for the 8088.

D140H-D143H IPC Read Register File  
(Read only)

These addresses are used to read from the IPC register file that can be written by the 8088.

D160H Clear Read Interrupt Request  
(Write only, don't care data)

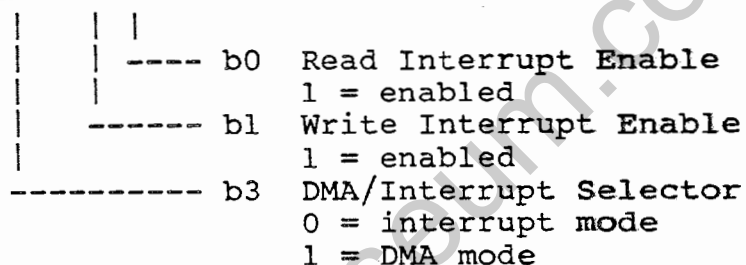
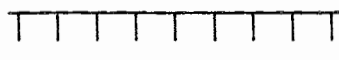
Writing any value to this location clears the Read Interrupt Request flag.

050H-053H Register File

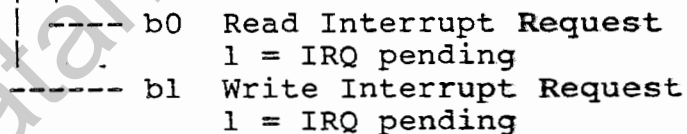
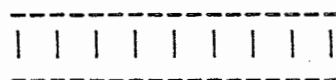
Reading from these locations accesses the register file that can be written by SALLY.

Writing to these locations writes into the register file that can be read by SALLY.

058H IPC Control Register  
WRITE



READ



Note: The main system PC board will allow the addresses on the 8088 side to be optionally (perhaps by cutting a trace and installing a jumper) moved up by 080H to the region of 0D0H-0DFH.



Appendix 1.4

SIO Software Logic Specification

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Appendix 1.5

Suggested Mechanical Line Drawings

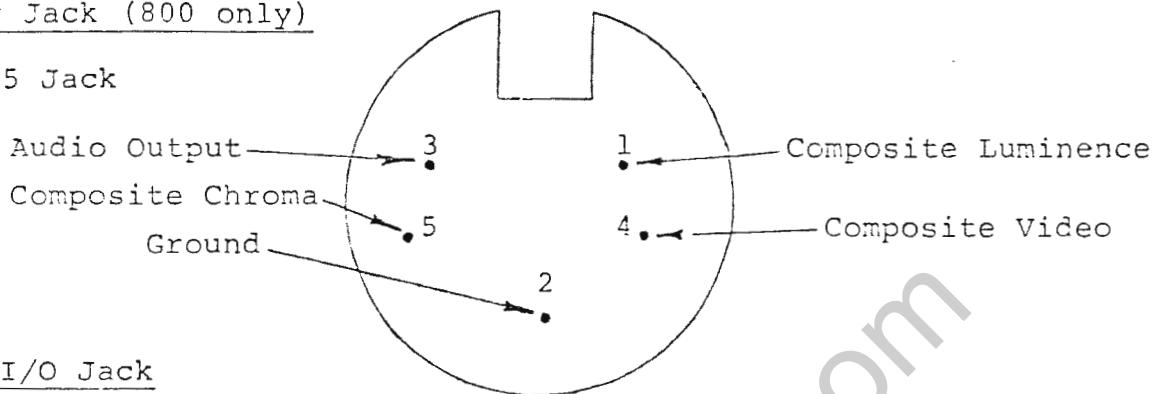
This Appendix consists of ~~three~~ sheets of suggested line drawings of the industrial design of the Atari 25601. These drawings are intended to show the preferred locations of the connectors and interfaces. The suggested dimensions are also detailed. These drawings are only suggestions and are not intended to constrain the vendor to the details.

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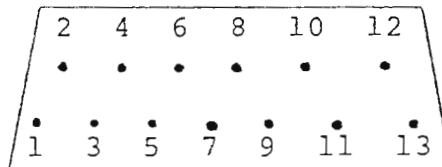
APPENDIX C: PINOUTS

Monitor Jack (800 only)

D.I.N. 5 Jack

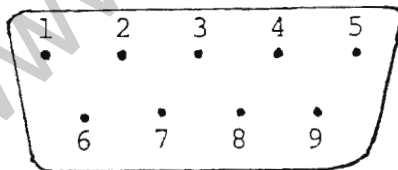


Serial I/O Jack



- |                 |                  |
|-----------------|------------------|
| 1. Clock Input  | 8. Motor Control |
| 2. Clock Output | 9. Proceed       |
| 3. Data Input   | 10. +5/Ready     |
| 4. Ground       | 11. Audio Input  |
| 5. Data Output  | 12. +12 volts    |
| 6. Ground       | 13. Interrupt    |
| 7. Command      |                  |

Controller Jack

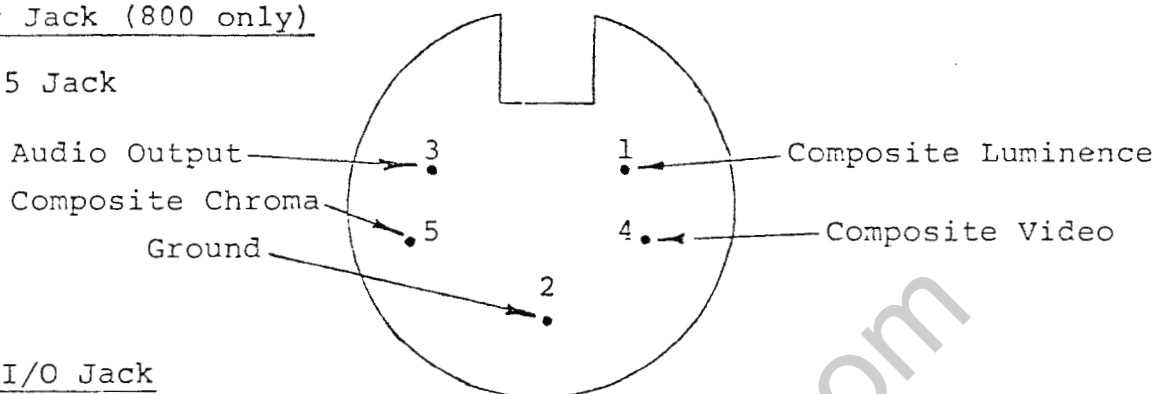


- |                             |                          |
|-----------------------------|--------------------------|
| 1. (Joystick) Forward Input | 6. Trigger Input         |
| 2. (Joystick) Back Input    | 7. +5 volts              |
| 3. (Joystick) Left Input    | 8. Ground                |
| 4. (Joystick) Right Input   | 9. A Potentiometer Input |
| 5. B Potentiometer Input    |                          |

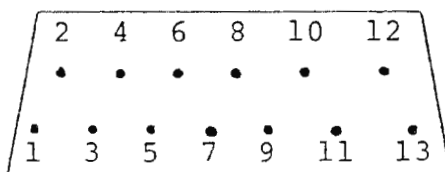
APPENDIX C: PINOUTS

Monitor Jack (800 only)

D.I.N. 5 Jack

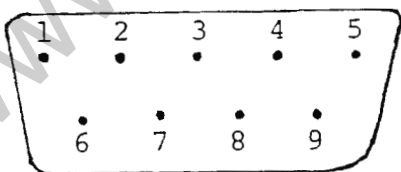


Serial I/O Jack



- |                 |                  |
|-----------------|------------------|
| 1. Clock Input  | 8. Motor Control |
| 2. Clock Output | 9. Proceed       |
| 3. Data Input   | 10. +5/Ready     |
| 4. Ground       | 11. Audio Input  |
| 5. Data Output  | 12. +12 volts    |
| 6. Ground       | 13. Interrupt    |
| 7. Command      |                  |

Controller Jack



- |                             |                          |
|-----------------------------|--------------------------|
| 1. (Joystick) Forward Input | 6. Trigger Input         |
| 2. (Joystick) Back Input    | 7. +5 volts              |
| 3. (Joystick) Left Input    | 8. Ground                |
| 4. (Joystick) Right Input   | 9. A Potentiometer Input |
| 5. B Potentiometer Input    |                          |