Amy STATUS 8/5/84

Sam NIGLIO

- ESTABLISH WEEKLY MEETINGS [redacted] ; DONE
  WITH CHIP GROUP (ASG) - SEE ATTACHED STATUS REPORTS

- DEBUG 2nd Amy BREADBOARD - PREP. ; DONE
  FOR TEST MODS (FOR USE IN SENTRY TEST DEVELOPMENT)

- COMPARE MOS (ODISY) AND BRBD (TTL) SCHEMATICS, ; DONE
  INPUT CHANGES TO ASG

- FINISH REV. C Amy SPEC ; DONE EXCEPT FOR Samp ϕ/16 TIMING DIAGRAM

- FIND MANPOWER TO DO PROPER ; DONE
  MOS SIMULATIONS OF THE FOLLOWING;
  1) RAMS
  2) ROMS
  3) CLOCK CIRCUITRY
  4) PRECHARGE ADDER
  5) INPUT ETF/F & SYNCHRONIZER

- GET Amy TEST PROGRAM STAFFED ; IN PROGRESS
  AND BRIEFED, UPDATE BRBD #2 FOR TESTING OF "TEST" BEFORE SILICON.

- HELP DEFINE SCORE & INSTRUMENT TABLE ; IN PROGRESS
  DATA FORMATS (INCLUDING INTERPOLATION)

- FINISH DRIVER (6301) FLOW CHARTS ; IN PROGRESS

- HELP DEFINE MUSIC EDITOR S/W & H/W ; IN PROGRESS

To: Sam Nicolino
From: Darryl Eng
Subject: AMY Status Report in Circuit Design Date: 7/31/84

Tasks for the week of 7/30/84 to 8/3/84

ENGINEERS	TASKS TO BE DONE
Sam Calpo Entered - PHASE RAM Starting - NOISE RAM	Work updating RAM and ROM logic/circuit diagrams, check the logic and timing of them and then run sc circuit simulation to verify. Provide layout device sizes for new modifications.
Chuck Hung NOT DONE	Work on clock buffer-precharge circuit simulations and will be using results to simulate RAM circuitr
John Mahoney DONE 3 IN PROGRESS	Work on Daisy to update logic diagram on the ROM portions so that the ROM coding can be implemented for NCC at later stage.
Darryl Eng	Work on ROM core programming for layout, check on clock/RAM/ROM logic/circuit. Aid layout with edits from first continuity check. Preparing plots for second continuity check and labeling text on pads for ERC and running NCC at later stage.

Colma - 2 Roms programmed

3 Roms being worked on

Inter Office Memo

Test Issues

ATARI®
Corporate Division

To: Sam Nicolino

From: Bob Hemming BH

Subject: AMY Progress Report Date: 7/30/84

Goals for week ending on August 7, 1984.

NCC conversion for AMY:

Hemming to finish this
2 large one's done
13 others being worked on

2 DONE 1) ROM coding will be completed on August 3, 1984 by John Mahoney.

DONE 2) RAM decoder and RAM core cell conversion will be completed on August 5, 1984 by Delwin Persson.

Tues. 3) Update logic on Daisy from finalized logic in 2 days after receiving signed-off logic from Sam Nicolino. Logic update will be done by Bob Hemming.

Silos test vector generation:

I) Sin and exp. ROM test vector done by August 3, 1984 by Bob Hemming. Finial pattern will be generated from net list exacted from final Daisy logic diagrams.

cc: Roland Ernst
Carl Nielsen

BH/bjk

TO: SAM [illegible]
FROM: DAVID EASTMAN
SUBJECT: AMY STATUS IN THE LAYOUT GROUP

CURRENTLY FOUR PEOPLE IN THE LAYOUT DESIGN ARE WORKING FULL TIME TO GET THE EDITS AND CHANGES THAT WERE FOUND IN THE FIRST AMY CONTINUITY CHECK. THE SCHEDULE THRU 8/10/84 IS AS FOLLOWS.

TASK	ESTIMATED DATE	PERSONNEL
START COLORING SECOND CONTINUITY PLOTS	8/1/84	DAVE EASTMAN
FINISH FIRST CONTINUITY EDITS	8/2/84	ADRIAN DAVIS TERRY SCOTT STEVE KIMURA THERESA ADSIT
START DRC RUN	8/2/84	ADRIAN DAVIS
START SECOND CONTINUITY CHECK (2A)	8/3/84	STEVE KIMURA
FINISH COLORING SECOND CONTINUITY PLOTS	8/3/84	DAVE EASTMAN TERRY SCOTT
START DRC EDITS	8/3/84	ADRIAN DAVIS TERRY SCOTT THERESA ADSIT
START SECOND CONTINUITY EDITS (2A)	8/7/84	ADRIAN DAVIS TERRY SCOTT THERESA ADSIT
START SECOND CONTINUITY CHECK (2B)	8/8/84	TERRY SCOTT THERESA ADSIT

1) Amy
2) NCR

To: Sam Nicolino
Fm: Lyle Supp
Subject: AMY Data Sheet
Date: 7/30/84

The AMY data sheet was delivered to you about 2 weeks ago for your correction. I have yet to recieve your updates. The Rev. A version (current), has been in the update mode for over 3 months. George Wang finished one set of revisions on 6/1/84. I plan no action on updating this spec until you have sent to me the marked up version which I gave you. After I receive your revised copy, I will then give you an estimate on when the spec will be completed.

CC: Carl Nielsen