ELECTRICAL APPLIANCE CONTROL - TRANSMITTER CHIP NO 542C

FEATURES

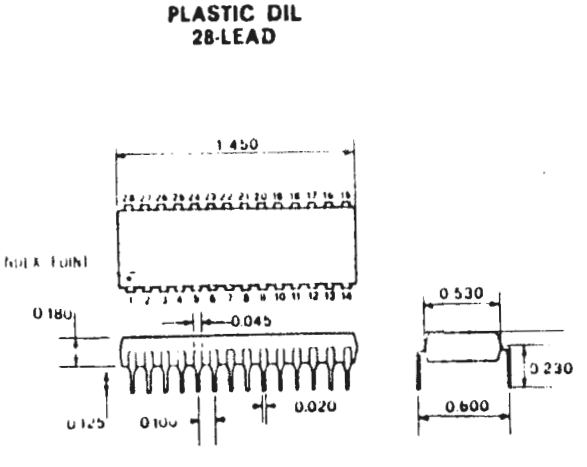
* OUTPUT CODE SYNCHRONIZED WITH LINE FREQUENCY
* OPERATES ON SINGLE OR THREE PHASE
* PARALLEL OR SERIAL DATA ENTRY
* 4 BIT SECURITY CODE
* HIGH NOISE IMMUNITY

DESCRIPTION

The transmitter circuit 542C is constructed on a monolithic chip utilising MOS P channel enhancement mode transistors. The circuit is primarily designed for use as a transmitter in a remote control system for electrical appliances and lighting using modules type X10-01460l/X10-01450l/X10-01470l as receivers.

Instructions from a 4 line code and a 4 x 8 matrix, (or a serial input), are converted to a 9 bit code suitably timed for transmission on the main a.c. power line. Using this code up to a maximum of 32 commands can be transferred to the a.c. line through external circuitry. By means of the 4 line security code up to 16 systems can operate independantly within the same electrical circuit.

PACKAGE INFORMATION



Pin	Function	Pin	Function
1	Strobe $\overline{S1}$	15	Serial Output
2	LED Output	16	K8
3	VDD	17	K7
4	VDD	18	K2
5	ØR Clock	19	K6
6	ØL Clock	20	K3
7	Serial Input	21	K1
8	Security H1	22	K4
9	Security H2	23	K5
10	Security H4	24	Strobe $\overline{S4}$
11	Security H8	25	Strobe $\overline{S2}$
12	Trigger	26	N/C
13	Option 50/60Hz	27	N/C
14	VSS	28	Strobe $\overline{S3}$

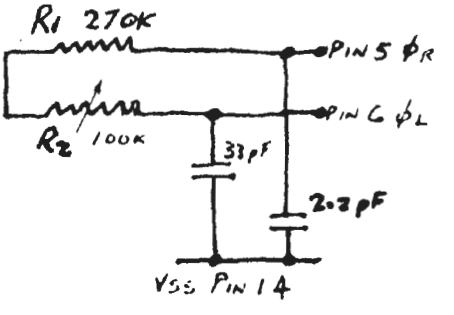
MAXIMUM RATINGS

VDD and Input Voltages (with respect to VSS = 0V)	-20V	to	+0.3V
Storage temperature	-50°C	to	+125°C
Operating temperature	0	to	+ 50°C

Electrical Characteristics	Min	Typ	Max	Units	Conditions
Supply Voltage VDD	-14.5		-18	V	
Current input IDD		6.0	7.0	mA	VDD = -18V
Frequency (Strobe output)	3.744	3.781	3.82	Khz	Measured on Pin 1
Data inputs K1 - K8 H1, H2, H4, H8, Ser. Input					
Logic '1'	-2		0	V	
Logic '0'	VDD		-8	V	
Strobe outputs					
Logic '1'	-1			V	
Logic '0'			-9	V	
LED Output					
Ron (Referenced to VSS)			500	Ω	V out = -2V
Roff(" " ")	1			MΩ	V out = -15V
Serial output					
Ron (Referenced to VSS)			400	Ω	V out = -2V
Roff (Referenced to VSS)	1			MΩ	V out = -15V
Line Trigger Input					
Logic '1'	-4			V	
Logic '0'			-5V		

OSCILLATOR

The oscillator is on board the chip, but requires two external capacitors and timing resistors to set the correct frequency.



Set frequency of S1 to 3.781Khz ± 1% by adjusting R2. This gives 121KHz data bursts at serial output (Pin 15).

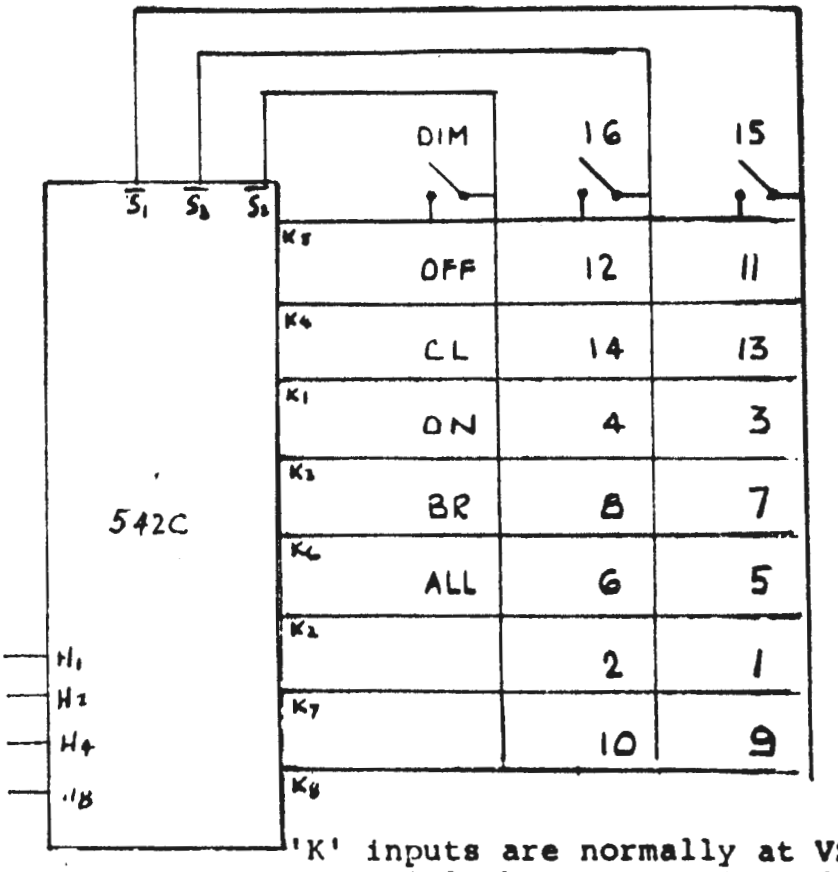
MODE OF OPERATION

DATA INPUT:

The 4 x 8 Matrix and the 4 line security inputs are ideally suited for inputing instructions using a Keyboard and a code switch. It is also possible to use these inputs to interface with a micro-computer.

SECURITY CODE DATA INPUT
(POSITIVE LOGIC)

STATE	H8	H4	H2	H1
A	1	0	0	1
B	0	0	0	1
C	1	1	0	1
D	0	1	0	1
E	1	1	1	0
F	0	1	1	0
G	1	0	1	0
H	0	0	1	0
I	1	0	0	0
J	0	0	0	0
K	1	1	0	0
L	0	1	0	0
M	1	1	1	1
N	0	1	1	1
O	1	0	1	1
P	0	0	1	1



'K' inputs are normally at VSS potential when not activated.

Figs. 2,3 & 4 show waveforms internal to the 542C chip. These waveforms help to explain the timing of the data from the "K" lines and the subsequent transmission of the serial output. Because the full transmission time takes 0.4 seconds to complete, a two stage buffer store is incorporated on the chip to enable data to be entered into the INPUT REGISTER whilst other data is being transmitted from the TRANSMISSION REGISTER. Once a key is depressed ("K" and "S" activated) the signal "LOCKOUT" is generated which inhibits any further entry into the INPUT REGISTER for a period of up to 8.3mS. The timing waveforms of Fig 2 show the sequence of signals for entering keyboard data for a key enabled by S3 strobe.

MODE OF OPERATION (Continued)

SERIAL INPUT:

Data inputing is also possible using the serial input (Pin 7). In System X10 this input is used to control the command console from a cordless remote control via an ultrasonic link.

The 542C serial input is designed to receive a self clocking message containing 5 digits, transmitted first in a true then in inverse form. Each transmission is made up of groups of 40Khz the length of each group determining a logic '1' or a logic '0'.

'1' bit 160 pulses followed by 4mSec delay.

'0' bit 48 pulses followed by 6.8mSec delay.

Each message transmitted in true and inverse form is preceded by '1' bit, and followed by "END CODE". END CODE ≡ 480 pulses followed by 4mSec delay.

DATA FORMAT: SEE FIG 5.

'1' bit ⟷ 8MSec	D8	D4	D2	D1	D16	$\overline{D8}$	$\overline{D4}$	$\overline{D2}$	$\overline{D1}$	$\overline{D16}$	End Code

The 542C is able to decode a message of the above format with a considerable tolerance on the number of pulses received and the delay between each group of pulses.

'1' bit - recognized with a minimum 128 pulses
'0' bit - recognized with a minimum 24 pulses
End Code - recognized with a minimum 320 pulses

Delay between bits can be as short as 2.5mSec.

A.C LINE CONDUCTED SIGNALS

In order to synchronize the digitally encoded output from "Serial Out" with the 60Hz A.C line the "Trigger" input is used. This input has a switching threshold of approximately -4.5V and it is important to arrange the switching of this point to be within ±100μS of the zero crossing of the A.C. line signal.

The transmitted message is thus synchronous with line A.C., each bit is clocked on zero crossing. Each message contains 9 bits of information, 4 security code, 5 matrix code. Each message is transmitted in true and inverse form on successive ½ cycles of the A.C line signal.

To allow operation on 3 phase systems as well as single phase, each data bit is transmitted 3 times corresponding to phase angles $0, \frac{\pi}{3}, \frac{2\pi}{3}$, which coinsides with zero crossing of other phases in the system.

A '1' bit is 3 x 1mS bursts of 120KHz commencing approximately 200μS after the zero crossing of each of the phases. A '0' bit is no signal for that half cycle. To synchronise the receivers with the transmitter a "Start Code" consisting of 3 successive '1' bits followed by a zero bit is used. Thus a complete message takes 11 full cycles of the A.C. line to complete.

SECURITY CODES

STATE	H8	H4	H2	H1
A	0	1	1	0
B	1	1	1	0
C	0	0	1	0
D	1	0	1	0
E	0	0	0	1
F	1	0	0	1
G	0	1	0	1
H	1	1	0	1
I	0	1	1	1
J	1	1	1	1
K	0	0	1	1
L	1	0	1	1
M	0	0	0	0
N	1	0	0	0
O	0	1	0	0
P	1	1	0	0

KEY CODES (A.C LINE)

KEY	D8	D4	D2	D1	D16
1	0	1	1	0	0
2	1	1	1	0	0
3	0	0	1	0	0
4	1	0	1	0	0
5	0	0	0	1	0
6	1	0	0	1	0
7	0	1	0	1	0
8	1	1	0	1	0
9	0	1	1	1	0
10	1	1	1	1	0
11	0	0	1	1	0
12	1	0	1	1	0
13	0	0	0	0	0
14	1	0	0	0	0
15	0	1	0	0	0
16	1	1	0	0	0
CLEAR	0	0	0	0	1
ALL	0	0	0	1	1
ON	0	0	1	0	1
OFF	0	0	1	1	1
BR	0	1	0	0	1
DIM	0	1	0	1	1

SERIAL DATA FORMAT

1	2	3	4	5	6	7	8	9	10	11	
START	CODE	H8 $\overline{H8}$	H4 $\overline{H4}$	H2 $\overline{H2}$	H1 $\overline{H1}$	D8 $\overline{D8}$	D4 $\overline{D4}$	D2 $\overline{D2}$	D1 $\overline{D1}$	D16 $\overline{D16}$	CYCLES

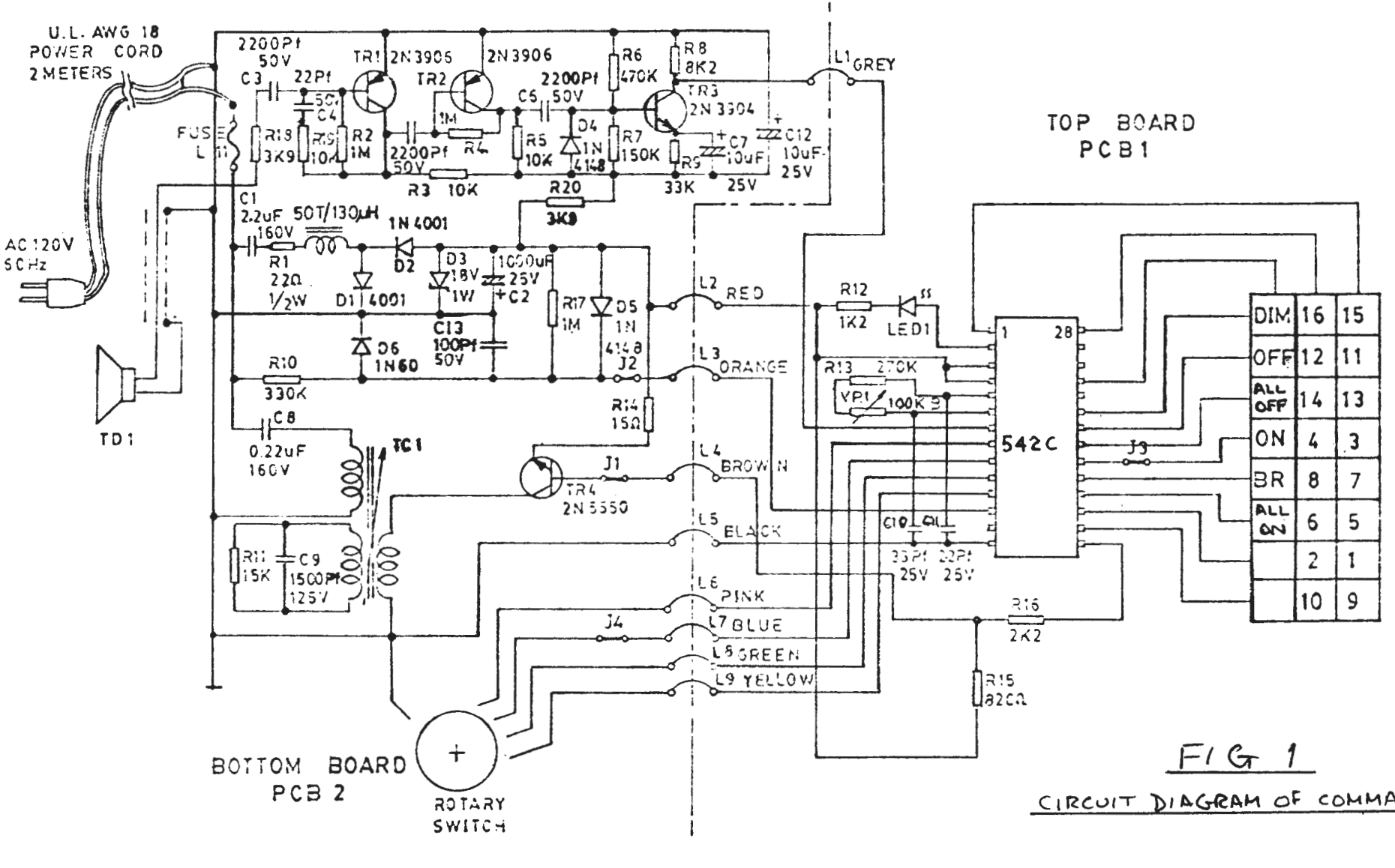


FIG 1

CIRCUIT DIAGRAM OF COMMAND CONSOLE

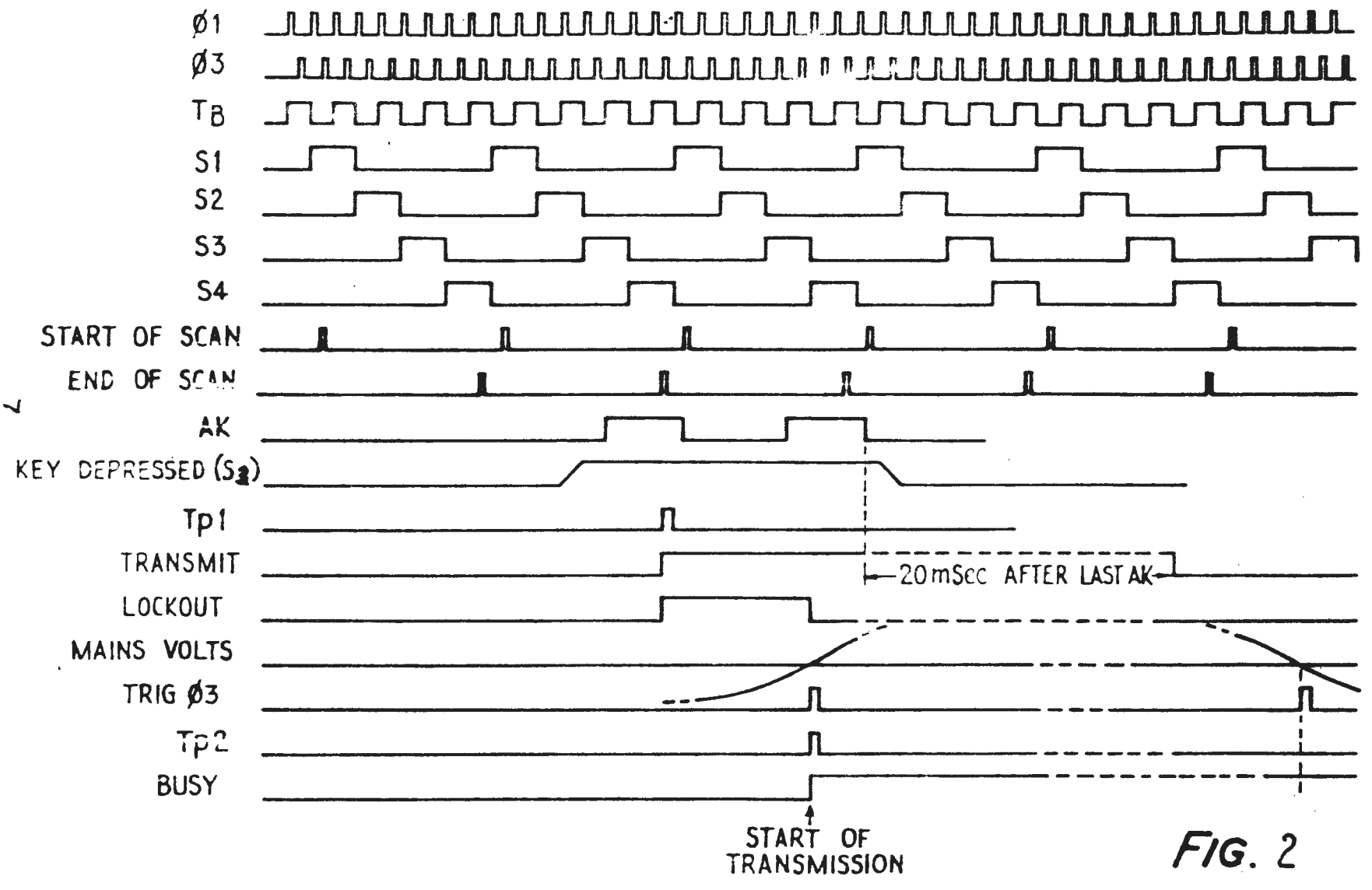

Ø1
Ø3
TB
S1
S2
S3
S4
START OF SCAN
END OF SCAN
AK
KEY DEPRESSED (S2)
Tp1
TRANSMIT
LOCKOUT
MAINS VOLTS
TRIG Ø3
Tp2
BUSY
20mSec AFTER LAST AK
START OF TRANSMISSION

FIG. 2

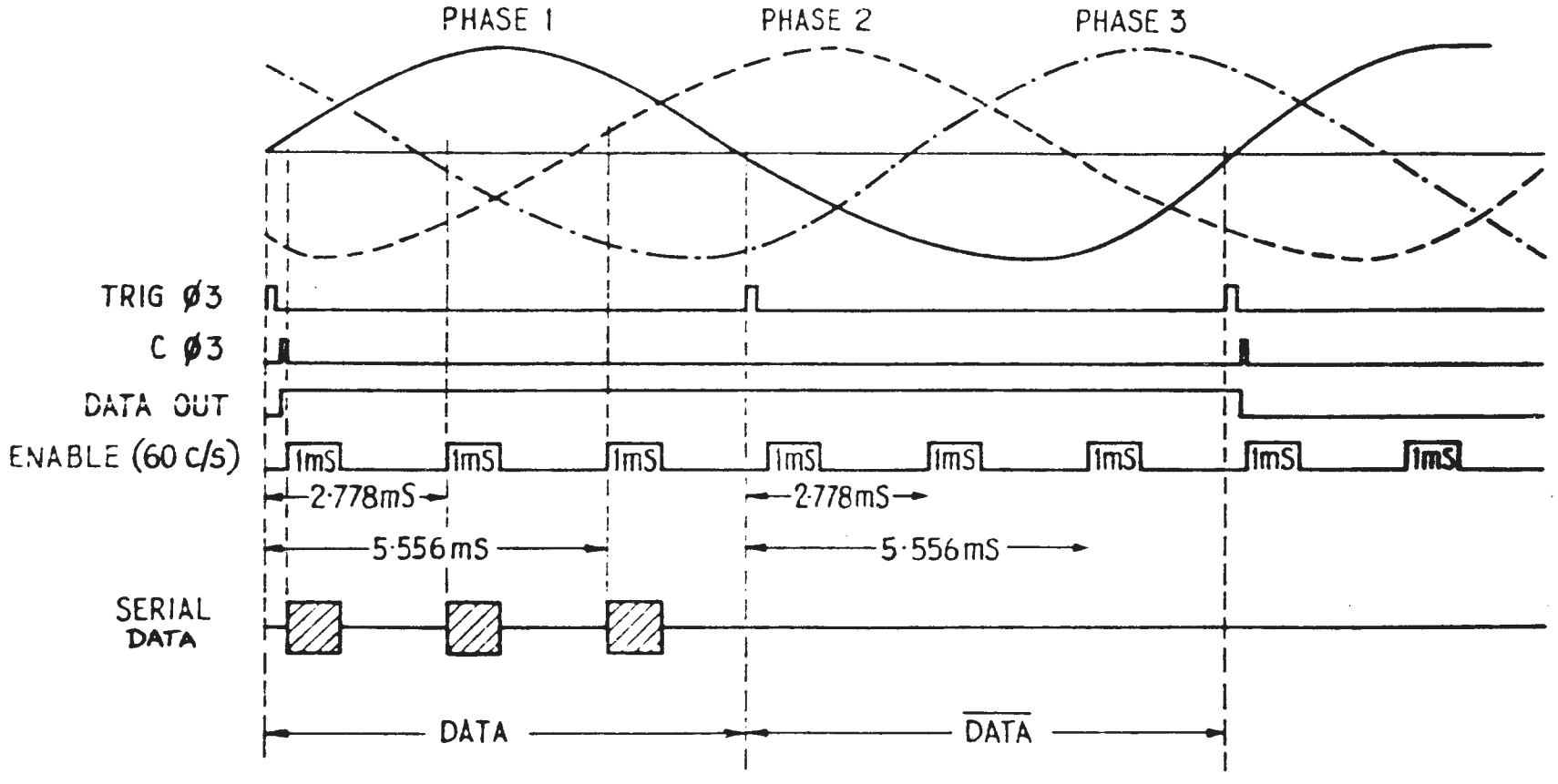

PHASE 1
PHASE 2
PHASE 3
TRIG ø3
C ø3
DATA OUT
ENABLE (60 c/s)
1mS
2·778mS
5·556mS
SERIAL DATA
DATA
DATA

FIG. 3

FIG 4 = CODE SENT FOR "DIM" ON HOUSE CODE 'P'

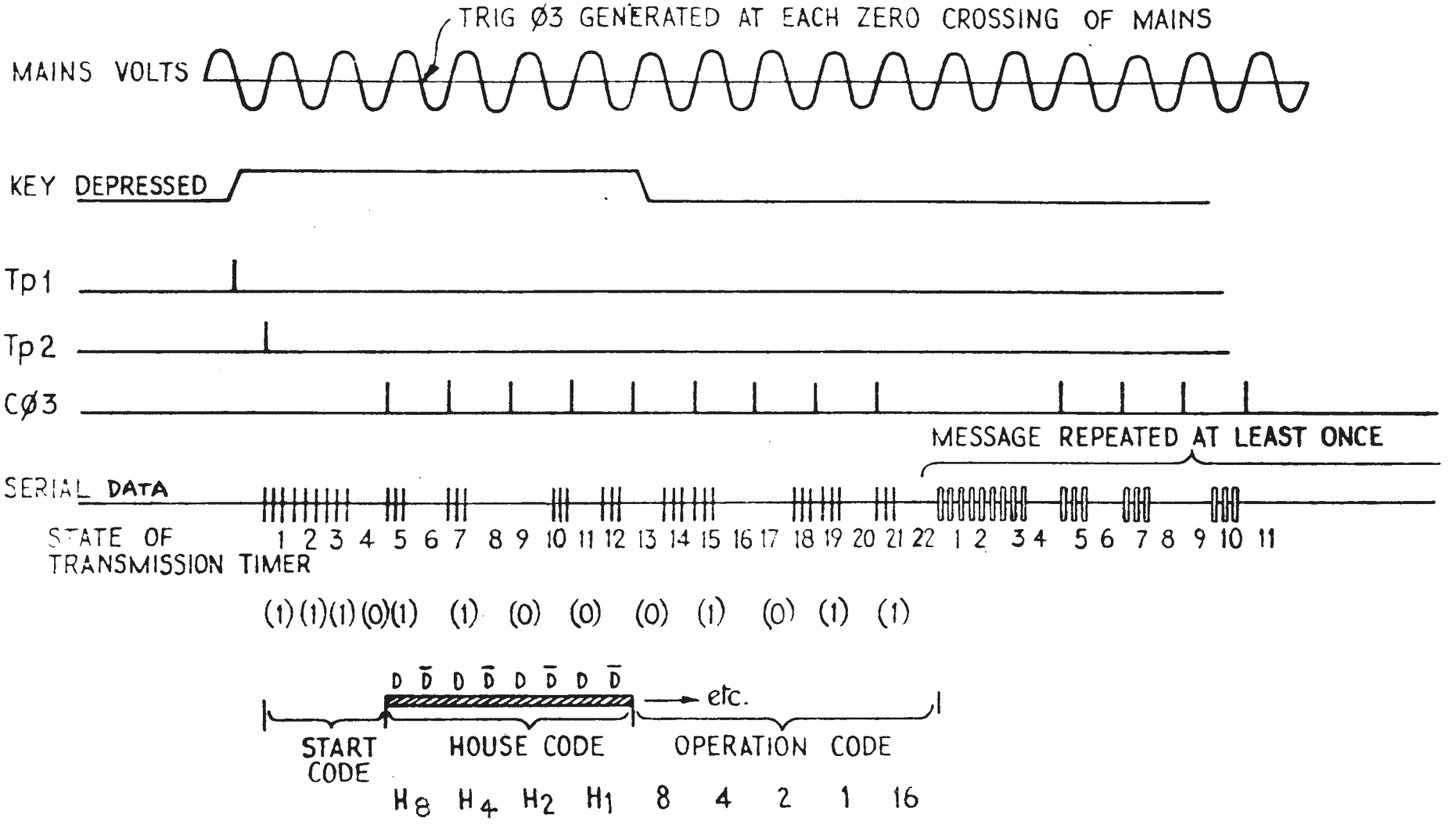
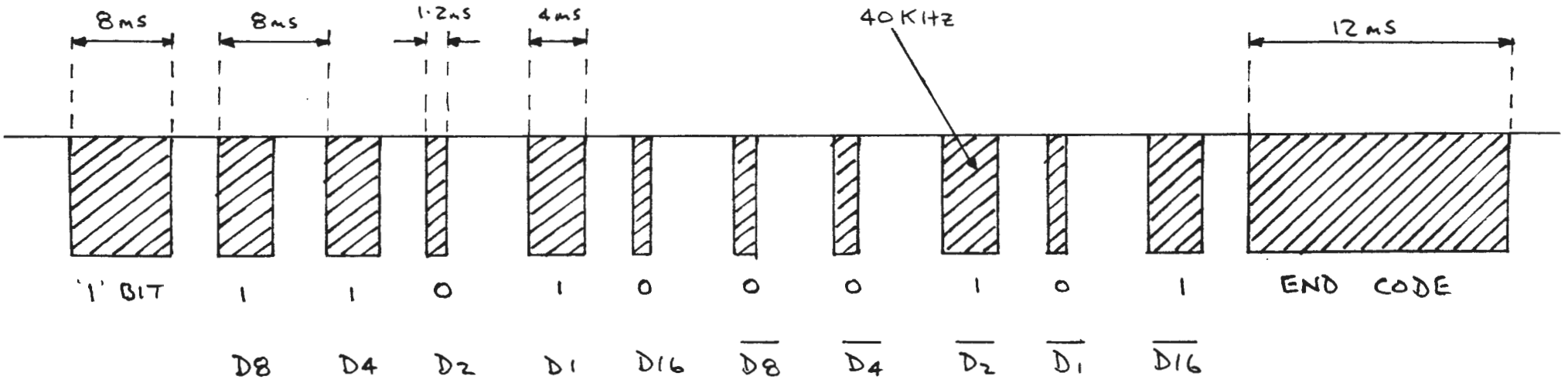


FIG 5



IN THIS EXAMPLE :- CODE SENT = 11010 = KEY '8'