PENNY1.ASG

INTEROFFICE MEMO
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SUBJECT: INITIAL PENNY CHIP PARTS ESTIMATE

The following is a minimal parts estimate for the internals of the PENNY chip. Note that the interface block (page 1) and control block (page 2) are both 'one time' only real estate requirements while the percept block (page 3) is to be repeated 32 times. For your assistance, I have included inter-percept bussing requirements (page 4). I would like your evaluation of the die size for a 32 percept PENNY chip as described on pages 1 through 4, plus the increase for the implimentation of option 1 (page 5), plus the increase for the implimentation of option 2 (also on page 5). If this information is insufficient, please get back to me as soon as possible. Thanks for your assistance.

INTERFACE BLOCK	QTY	DESCRIPTION
ADDRESS OUTPUT	8	DRIVERS (4 TTL LOADS EACH)
SELECT/RAS INPUT/OUTPUT	1	DRIVER (4 TTL LOADS)
CAS OUTPUT	1	DRIVER (4 TTL LOADS)
MEMORY MUX OUTPUT	1	DRIVER (4 TTL LOADS)
PROCESSOR WRITE OUTPUT	1	DRIVER (6 TTL LOADS)
COLOR OUTPUT	4	DRIVER (1 TTL LOAD EACH)
INTENSITY OUTPUT	4	DRIVER (1 TTL LOAD EACH)
PROCESSOR WRITE INPUT	1	GATE
DATA INPUT	16	16-BIT LATCH
CLOCK INPUT	1	8.87 MHz (PAL)
Vcc	1	VOLTS
Vss	1	GROUND
TOTAL	40	

CONTROL BLOCK	QTY	DESCRIPTION
MACRO CONTROL MACHINE	3	D-FLIP-FLOPS WITH CLEAR
	12	2-INPUT NAND GATES
ADDRESS CACHE	1	14-BIT PRESETABLE SYNCHRONOUS BINARY UP/DOWN COUNTER
	64	SIMPLE 14-BIT LATCHES
DATA ADDRESS MAPS	32	6-BIT SIMPLE LATCHES
MEMORY ACCESS MACHINE	2	D-FLIP-FLOPS WITH CLEAR
	8	2-INPUT NAND GATES
SELECT/MUX CONTROL	2	D-FLIP-FLOPS WITH CLEAR
	8	2-INPUT NAND GATES
PERCEPT SELECTOR	1	1 TO 32 DEMUX
INVERT SWITCH	32	1-BIT SIMPLE LATCHES
QUAD 4-BIT BIN-POLY CONVERTER	64	2-INPUT NAND GATES
COORDINATE COMPUTER	1	9-BIT ASYNCHRONOUS BINARY ADDER
PROCESSOR WRITE LOGIC	3	2-INPUT NAND GATES
COMPOSITE SYNC DETECTOR	1	DYNAMIC MEMORY CELL (450 ns DECAY TIME)
	1	D-FLIP-FLOP WITH CLEAR & PRESET
	4	2-INPUT NAND GATES
HSYNC GENERATOR	2	2-INPUT NAND GATES

SCREEN ENABLE LOGIC	3	D-FLIP-FLOPS WITH CLEAR
	1	D-FLIP-FLOP WITH PRESET
	6	2-INPUT NAND GATES
MISCELLANEOUS	5%	EXTRA STUFF I FORGOT (GATES, ETC.)

PERCEPT BLOCK	QTY	DESCRIPTION
PERCEPT ENABLE SWITCH	1	SIMPLE 1-BIT LATCH
MACRO CONTROL MACHINE	3	D-FLIP-FLOPS WITH CLEAR
	12	2-INPUT NAND GATES
PARAMETER SERVICE MACHINE	4	D-FLIP-FLOPS WITH CLEAR
	16	2-INPUT NAND GATES
DATA SERVICE MACHINE	2	D-FLIP-FLOPS WITH CLEAR
	8	2-INPUT NAND GATES
SERVICE PRIORITIZATION	24	2-INPUT NAND GATES
DISPLAY PRIORITIZATION	52	2-INPUT NAND GATES
PARAMETER CACHE	1	SIMPLE 9-BIT LATCH
	1	SIMPLE 8-BIT LATCH
	1	SIMPLE 6-BIT LATCH
FORMAT INTERPRETER	1	SIMPLE 7-BIT LATCH
	28	2-INPUT NAND GATES
GRAPHICS GENERATOR	3	1 TO 8 DEMUX
	10	4-BIT OPEN COLLECTOR GATES
	3	8-BIT OPEN COLLECTOR GATES
POLYCOUNTER SEEDS	4	SIMPLE 4-BIT LATCHES
REVERSE DATA SWITCH	1	SIMPLE 1-BIT LATCH
COLOR PRIORITY SWITCH	1	SIMPLE 1-BIT LATCH

MULTILINE SWITCH	1	SIMPLE 1-BIT LATCH
PROGRAMMABLE POLYCOUNTER ARRAY	16	PRESETABLE RIGHT SHIFT SYNCHRONOUS SHIFT-REGISTERS
	12	2-INPUT NAND GATES
ACTIVE PERCEPT DETECTOR	1	1 OF 32 DATA SELECTOR
MISCELLANEOUS	5%	EXTRA STUFF I FORGOT (GATES, ETC.)

COMMON PERCEPT BUSSES	QTY	DESCRIPTION
DISPLAY PRIORITY IN/OUT	13	OPEN COLLECTOR (8.87 MHz) BIDIRECTIONAL 13 OUTPUTS PER PERCEPT 13 INPUTS PER PERCEPT 13 INPUTS TO CONTROL
SERVICE PRIORITY IN/OUT	6	OPEN COLLECTOR (8.87 MHz) BIDIRECTIONAL 6 OUTPUTS PER PERCEPT 6 INPUTS PER PERCEPT 6 INPUTS TO CONTROL
DATA IN	16	DRIVEN (8.87 MHz) UNIDIRECTIONAL 16 INPUTS PER PERCEPT 16 OUTPUTS FROM CONTROL
SERVICE GRANT IN	1	DRIVEN (8.87 MHz) UNIDIRECTIONAL 1 INPUT PER PERCEPT 1 OUTPUT FROM CONTROL
PARAMETER STROBES IN	7	DRIVEN (8.87 MHz) UNIDIRECTIONAL 7 INPUTS PER PERCEPT 7 OUTPUTS FROM CONTROL
COLOR OUT	4	OPEN COLLECTOR (8.87 MHz) UNIDIRECTIONAL 4 OUTPUTS PER PERCEPT 4 INPUTS TO INTERFACE OUT

INTENSITY OUT		4 OPEN COLLECTOR (17.73 MHz) UNIDIRECTIONAL 4 OUTPUTS PER PERCEPT 4 INPUTS TO INTERFACE OUT
PERCEPT ACTIVE IN/OUT		32 DRIVEN (8.87 MHz) 1 OUTPUT PER PERCEPT 32 INPUTS PER PERCEPT
CLOCK IN	1	DRIVEN (8.87 MHz) 1 INPUT PER PERCEPT 1 OUTPUT FROM CONTROL
HSYNC (CLEAR)		1 DRIVEN (225 ns) 1 INPUT PER PERCEPT 1 OUTPUT FROM CONTROL
SCREEN ENABLE		1 DRIVEN (225 ns) 1 INPUT PER PERCEPT 1 OUTPUT FROM CONTROL

TOTAL INTERNAL BUS LINES		86

This is option 1. It adds the capability to generate 3-D surfaces.

PERCEPT BLOCK	QTY	DESCRIPTION
YAW GENERATOR	1	8-BIT PRESETABLE SYNCHRONOUS BINARY UP/DOWN COUNTER
	2	D-FLIP-FLOPS WITH CLEAR
	6	1 OF 32 DATA SELECTORS
	5	PRESETABLE RIGHT SHIFT SYNCHRONOUS SHIFT REGISTERS
	10	2-INPUT NAND GATES
	1	SIMPLE 5-BIT LATCH
YAW & PITCH CONTROLLER	3	D-FLIP-FLOPS WITH CLEAR
	2	SIMPLE 1-BIT LATCHES
	10	2-INPUT NAND GATES
Z-COORDINATE COUNTER	1	8-BIT PRESETABLE SYNCHRONOUS BINARY UP/DOWN COUNTER

This is option 2. It adds 5 binary points of internal resolution to z-coordinate surface generation.

PERCEPT BLOCK	QTY	DESCRIPTION
HIGH RES DISPLAY PRIORITY	20	2-INPUT NAND GATES
	1	5-BIT PRESETABLE SYNCHRONOUS BINARY UP/DOWN COUNTER

COMMON PERCEPT BUSSES	QTY	DESCRIPTION
HIGH RES DISPLAY PRIORITY I/O	5	OPEN COLLECTOR (8.87 MHz) BIDIRECTIONAL 5 OUTPUTS PER PERCEPT 5 INPUTS PER PERCEPT 5 INPUTS TO CONTROL
TOTAL ADDITIONAL BUS LINES	5	