VIVIAN1.ASG

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TO:
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SUBJECT: INITIAL VIVIAN CHIP PARTS ESTIMATE

The following is a minimal parts estimate for the internals of the VIVIAN chip. Note that the interface block (page 1) and control block (page 2) are both 'one time' only real estate requirements while the associative array and attributes block (page 3) can be repeated up to 16 times. I would like your evaluation of the die size for a 16 associative array VIVIAN chip as described.

Also estimate should be made on the 10 bit associtive array with the associated masking and attribute circuitry so one can reduce the die be scaling back on the number of chip selects.

INTERFACE BLOCK	QTY	DESCRIPTION
ADDRESS INPUT	8	8-BIT LATCH
RAS* INPUT/OUTPUT	16	DRIVER (4 TTL LOADS)
CAS OUTPUT	1	DRIVER (4 TTL LOADS)
ADDRESS MUX OUTPUT	1	DRIVER (4 TTL LOADS)
PROCESSOR WRITE OUTPUT	2	DRIVER (6 TTL LOADS)
PROCESSOR WRITE INPUT	1	GATE
DATA INPUT	4	4-BIT LATCH
CLOCK INPUT	1	8.87 MHz (PAL)
Vcc	1	+5 VOLTS
Vss	1	GROUND
TOTAL	40	

CONTROL BLOCK	QTY	DESCRIPTION
MACRO CONTROL MACHINE		D-FLIP-FLOPS WITH CLEAR
	2	2-INPUT NAND GATES
DATA ADDRESS MAPS	32	6-BIT SIMPLE LATCHES
MEMORY ACCESS MACHINE	2	D-FLIP-FLOPS WITH CLEAR
	8	2-INPUT NAND GATES
SELECT/MUX CONTROL	2	D-FLIP-FLOPS WITH CLEAR
	8	2-INPUT NAND GATES
INVERT SWITCH	32	1-BIT SIMPLE LATCHES
QUAD 4-BIT BIN-POLY CONVERTER	64	2-INPUT NAND GATES
PROCESSOR WRITE LOGIC	3	2-INPUT NAND GATES
COMPOSITE SYNC DETECTOR	1	DYNAMIC MEMORY CELL (450 ns DECAY TIME)
	1	D-FLIP-FLOP WITH CLEAR & PRESET
	4	2-INPUT NAND GATES
HSYNC GENERATOR	2	2-INPUT NAND GATES
SCREEN ENABLE LOGIC	3	D-FLIP-FLOPS WITH CLEAR
	1	D-FLIP-FLOP WITH PRESET
	6	2-INPUT NAND GATES
MISCELLANEOUS	5%	EXTRA STUFF I FORGOT (GATES, ETC.)

ASSOCIATIVE BLOCK	QTY	DESCRIPTION
MACRO CONTROL MACHINE	3	D-FLIP-FLOPS WITH CLEAR
	12	2-INPUT NAND GATES
PARAMETER SERVICE MACHINE	4	D-FLIP-FLOPS WITH CLEAR
	16	2-INPUT NAND GATES
DATA SERVICE MACHINE	2	D-FLIP-FLOPS WITH CLEAR
	8	2-INPUT NAND GATES
SERVICE PRIORITIZATION	24	2-INPUT NAND GATES
MISCELLANEOUS	5%	EXTRA STUFF I FORGOT (GATES, ETC.)

BUSSES	QTY	DESCRIPTION
DATA IN	16	DRIVEN (8.87 MHz) UNIDIRECTIONAL 16 INPUTS PER PERCEPT 16 OUTPUTS FROM CONTROL
CLOCK IN	1	DRIVEN (8.87 MHz) 1 INPUT PER PERCEPT 1 OUTPUT FROM CONTROL
HSYNC (CLEAR)	1	DRIVEN (225 ns) 1 INPUT PER PERCEPT 1 OUTPUT FROM CONTROL
TOTAL INTERNAL BUS LINES	86	

This is option 1.

This is option 2.

This is option 3.