VIVIAN FUNCTIONAL SPECIFICATION

1. INTRODUCTION

Vivian is a memory management unit that is configured at power up to allow basic architecture to handle a broad mix of memory and I/O configuration and timing. Vivian provides controls for both address translation and memory overlay. It also can select two separate blocks of memory to implement efficient DMA with CPU acting as a DMA controller, and refresh the dynamic RAMs in the system.

1.1 MEMORY BLOCKS

The Vivian partitions the 16M address space into 1024 blocks of 16k words each. After initialization Vivian can translate 16 of the 1k block address into 16 actual physical blocks. By masking out some of the bits of the block address, the physical block address can be further expanded by an external decoder.

1.2 PROGRAMMING VIVIAN

Vivian is programmed at power up to map logical address blocks to physical address blocks. There is also a mask option to mask out a number of block address bits which can then be expanded by an external decoder. Associated with each physical block are two attributes; configuration and timing. The configuration attribute specifies the type of peripheral on the physical block, i.e. ROM, DRAM, I/O. The timing attribute specifies the read-write speed associated with each of the physical blocks. If a physical block is expanded , then each of the expanded

blocks must share the same attributes. When Vivian is programmed for the COPY mode, it simultaneously enables one physical block as the write block and another as the read block thus allowing the CPU to DMA in one instruction cycle.

1.3 ADDRESS TRANSLATION

The address translation is done by 16 x 10 associative memory which is programmed during initialization. Under normal translation the logical block address provided by the CPU is associatively decoded to one of sixteen physical block address and the associated configuration and timing attributes are also enabled. If the expanded addressing is used then some of the bits of the logical block address is masked as 'don't care' by Vivian and is decoded externally to select the expanded number of blocks.

1.4 PHYSICAL BLOCK CONTROL

The RAS* chip select outputs can function in a multitude of ways depending on the configuration mode, i.e. aside from the normal chip select it can also be asynchronous and/or bidirectional. If the chip select of Vivian is configured to be bidirectional an external device can assert RAS* and take over the control of the associated physical memory block. The arbitration protocol is handled by the hardware in Vivian. At any given time any number of devices may simultaneously access their associated physical memory block.

1.5 DMA CONTROL

When Vivian is set in the Copy mode, two RAS* are enabled one for the READ block and the other for the WRITE block. The CPU stores the DMA starting address and the DMA word count. VIVIAN also has two R/W* lines, each controlling a disjoint set of physical blocks.

1.6 MEMORY REFRESH CONTROL

The HSYNCH input to the VIVIAN initiates memory refresh which does four rows of refresh for every HSYNCH signal. Since the HSYNCH occurs every 64 microseconds, 256 rows are refreshed every 4 milliseconds.

2. VIVIAN SIGNAL DESCRIPTION

This section contains a brief description of the input and output signals. Pin count and input output designations are given below.

	1. VCC		
	2. GND		
	3. AD	(10)	Input
	4. DAT	(4)	Input
	5. AS*		Input
*	6. DS*		Input
	7. DTACK		Output
	8. RAS*	(16)	Input/Output
	9. CAS*		Output
*	10. DCAS		Output
	11. CLK		Input
*	12. HSYNCH		Input
	13. R/W*		Input
	14. CR/W*	(2)	Output
	15. RFSH		Output
	TOTAL PINS	40-43	

(PINS WITH * ARE SIGNALS THAT COULD BE GENERATED EXTERNALLY)

2.1 VCC

The VCC supplies power to Vivian at +5 volts.

2.2 GND

The GND is connected to the system ground.

2.3 ADDRESS (AD1-AD10)

The most significant ten bits of the CPU address which corresponds to AD14-AD23 of the 24 bit CPU address.

2.4 DATA (DAT0-DAT3)

The least significant 4 bits of the CPU data which corresponds to D0-D3 of the 8 bit data.

2.5 ADDRESS STROBE (AS*)

This input signal indicates to Vivian that a bus cycle is in progress and that a valid address is on the address bus. The assertion of AS* initiates the normal translation phase of the bus cycle and the assertion of the RAS* signal.

2.6 DATA STROBE (DS*)

The DS* input is used during write operation to the Vivian. The data strobe indicates to Vivian that valid data is on the data bus. DS* corresponds to LDS* for a multiplexed data.
(DS* is not required if the time for the valid data can be derived.)

2.7 DATA TRANSFER ACKNOWLEDGE (DTACK*)

Vivian uses this rescindable output to signal the completion of the operation phase of the bus cycle to the processor. If the bus cycle is processor read, the Vivian asserts DTACK* to indicate that the information on the data bus is valid. If the bus cycle is processor write to the Vivian, DTACK* is used to acknowledge acceptance of the data by the Vivian. The output is open drain so the line can be wired-ORed with DTACK* from other devices, and VIVIAN also uses the pin as an input to detect the end of an asynchronous data transfer cycle.

2.8 ROW ADDRESS STROBE (RAS*1-RAS*16)

This bidirectional pin functions as chip select by the Vivian and is also used to latch the row address into the bank of DRAMs selected. On refresh cycle all the RAS* for the physical blocks with DRAMs are active. When these pins receive RAS* from an external device, VIVIAN relinquishes the control of the selected memory block to the external device.

2.9 COLUMN ADDRESS STROBE (CAS*)

This output is used as the multiplex signal to select the row and column address of a DRAM array.

2.10 DELAYED COLUMN ADDRESS STROBE (DCAS*)

This output is used to latch the column address into the DRAM array.
(DCAS* may be derived from CAS* externally.)

2.11 SYSTEM CLOCK (CLK)

This input provides master timing to generate the RAS*-CAS* timing of the Vivian.

2.12 HORIZONTAL SYNCH (HSYNCH)

The horizontal synch input comes from the video generator chip and corresponds to the TV's line frequency. Vivian initiates the four lines of refresh cycle on the trailing edge of this signal.
(HSYNCH signal may be obviated if the CLK signal is altered during the horizontal synch period and then have VIVIAN detect the the alteration, i.e. a dynamic cell to sense the duty cycle of the CLK signal.)

2.13 READ/WRITE (R/W*)

This input signal defines the data bus transfer as a CPU read or write cycle.

2.14 CONTROLLED READ/WRITE (CR/W1*,CR/W2*)

These outputs each controls the read/write for number of disjoint set of physical blocks.

2.15 REFRESH (RFSH)

This signal controlls the refresh counter and the address multiplexer for the refresh cycle.

3. VIVIAN REGISTER DESCRIPTIONS

The following table shows the programming model of Vivian. The Vivian registers consists of associative memory array, mask registers, attribute registers, and DMA control registers.

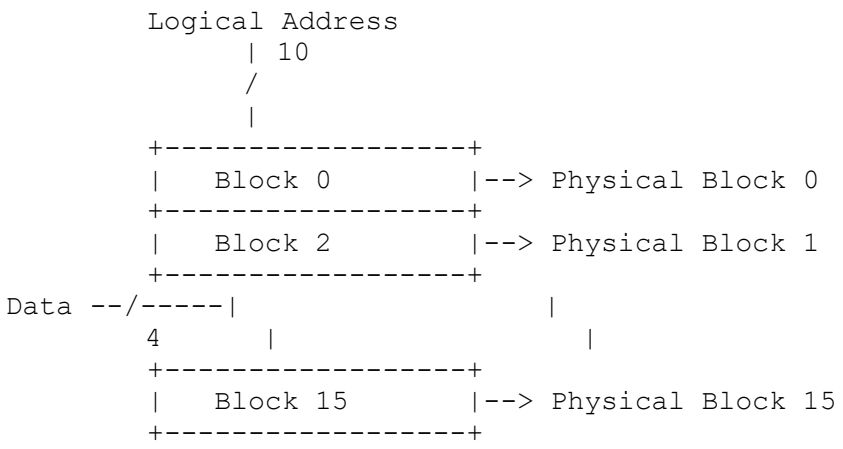
R/W	BLKADR	DATA	MODE	COMMENT
R	%	%	%	Normal read cycle.
W	>0	%	NORM	Normal write cycle.
W	0	m	%	Set mode.
W	l	p	MAP	Map LOGICAL_BLOCK(l) to PHYSICAL_BLOCK(p).
W	m	p	MASK	Masks number of bits of the logical block.
W	c	p	CONF	Configure PHYSICAL_BLOCK(p) per configuration word c.
W	t	p	TIME	Set timing for PHYSICAL_BLOCK (p) per timing word t.
W	l	*	COPYID	Identify LOGICAL_BLOCK(l) as the source block.
W	l	*	COPY	DMA copy from source block to LOGICAL_BLOCK(l)

l,c,t>0 are 10bits m=0 reset m=3 configuration
m,p are 4 bits m=1 map m=4 timing
% is don't care m=2 mask m=5 copyid
* CPU data tri-state m=6 copy

3.1 ASSOCIATIVE ARRAY

The associative array is programmed during initialization using the four bit data to select the 16 associative memory array and the ten bit address as data to be written into the

selected memory address. After the initial set up, subsequent address on the ten bit block address will be mapped into one of sixteen physical blocks.

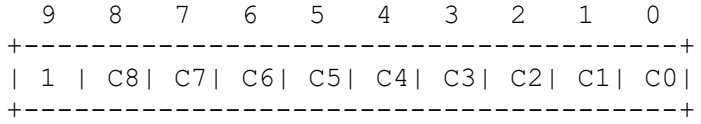


3.2 MASKED ASSOCIATIVE ARRAY

If any physical block is to be expanded to additional physical blocks, then some of the bits of the logical block address corresponding to the physical block of Vivian are masked. The masking is accomplished by programming the mask registers under MASK mode. There is a ten bit register for each word of the associative memory which, if set, masks out the corresponding bit of the associative memory. The masked bits of the block address can then be expanded by an external decoder. If an external decoder is not used, the logical block address will be multiply mapped throughout the masked address space.

3.3 CONFIGURATION REGISTER

The configuration attributes are stored in 16 ten bit registers, one for each physical block address. During set up the four bit data line selects one of sixteen registers, and the the ten bit address line holds the configuration attribute. Operationally, the registers are selected by the associative memory row that matches the logical block address. Then the configuration attributes are decoded to control the RAS*-CAS* lines. Each of the configuration registers is set as follows:

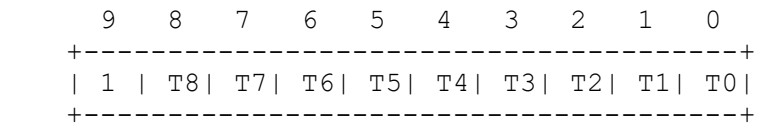


C0: 0 READ_ONLY_BLOCK
1 READ_WRITE_BLOCK

```
C1:   0     RAS*_OUTPUT_BLOCK
      1     RAS*_BIDIRECTIONAL_BLOCK

C2:   0     NON_DYNAMIC_MEMORY
      1     DYNAMIC_MEMORY

C3:     0       SYNCHRONOUS BLOCK
      1     ASYNCHRONOUS BLOCK

C4-C8:           NOT DEFINED
```

3.4 TIMING REGISTER

The timing attributes are stored in 16 ten bit registers, one for each physical block address. During set up the four bit data line selects one of sixteen registers, and the the ten bit address line holds the timing attribute. Operationally, the registers are selected by the associative memory row that matches the logical block address. Then the timing attributes are decoded to control the RAS*-CAS* lines. Each of the timing registers is set as follows:



T0-T3: WAIT STATES FOR MEMORY ACCESS

T3-T8: NOT DEFINED

3.5 COPY (DMA) REGISTER

When the COPY mode is enabled the contents of the physical READ block identified by the four bit data line is copied into physical WRITE block which is block mapped from the address on the ten bit logical address line. The two R/W* lines select the READ block and the WRITE block from two disjoint set of physical blocks, so even a RAM can be selected as a READ block simultanenously with a WRITE block. The CPU acts as the DMA controller with starting address and DMA block length stored in the CPU registers.

3.6 VIVIAN PROGRAMMING

The following is an example of Vivian programming:

1. SET MODE

```
LOAD  R2,#0
LOAD  R1,#M ;M=MODE:0-7
STORE (R2),R1
```

2. MAP MODE

```
LOAD  R2,#L ;L=LOGICAL_BLOCK:1-1024
LOAD  R1,#P ;P=PHYSICAL_BLOCK:1-15
STORE (R2),R1
```

3. MASK MODE

```
LOAD  R2,#M ;M=LOGICAL_BLOCK_MASK:>0
LOAD  R1,#P ;P=PHYSICAL_BLOCK:1-15
STORE (R2),R1
```

4. TIMING/CONFIGURATION MODE

```
LOAD  R2,#A ;A=TIMING_WORD,CONFIG_WORD:>0
LOAD  R1,#P ;P=PHYSICAL_BLOCK:1-15
STORE (R2),R1
```

5. COPY MODE

```
LOAD  R2,#R ;R=READ_BLOCK:0-15
LOAD  R1,#W ;W=WRITE_BLOCK:1-1024
STORE (R2),R1
```

```
LOAD  R2,#S ;S=DMA_START_ADDRESS
LOAD  R1,#C ;C=DMA_WORD_COUNT
;LOOP
```

4. VIVIAN FUNCTIONAL DESCRIPTION

4.1 ASSOCIATIVE ARRAY

The associative array consists of 16 words of ten associative cells which are simply a latch to hold one bit of data and an Exclusive-OR gate which compares the content of the latch with the current data line. The outputs of the EX-OR gate are wired-ORed for each ten bit word to enable the chip select for the selected physical block address. The address '0' is reserved for the operating system and translates to physical block address '0'. The physical block '0' chip select disables the other 15 chip selects.

4.2 MASKED OPTION

When some of the bits of logical block address is masked by the associated mask register, the physical block selected can be expanded to 2^N additional physical blocks, where N is the number of masked bits. The masked bits are decoded by an external decoder to expand the chip select to the additional blocks. The timing and configuration attributes are the same for the expanded blocks.

4.3 CONFIGURATION ATTRIBUTE

The configuration register is decoded to control the RAS* and CAS* line for the associated physical block. During a memory refresh all the RAS* line for the DRAM's are activated. Also input function of the RAS* line is disabled for the physical blocks without address overlays. The configuration attribute also defines four modes of peripheral control.

4.4 TIMING ATTRIBUTE

The timing register bits T0-T3 allows the matching of a synchronous physical block to the system access time by inserting a corresponding number of clocks as wait states. The timing attribute is ignored for an asynchronous physical block.

4.5 DMA CONTROL

DMA is done by using the CPU as a DMA controller while VIVIAN is used to select the READ_BLOCK and the WRITE_BLOCK simultaneously. VIVIAN has two separate R/W* output lines so at any given time one block can act as the READ block and another as the WRITE block. One block cannot be simultaneously be a READ block and a WRITE block. The timing defaults to slower of the two selected physical blocks.

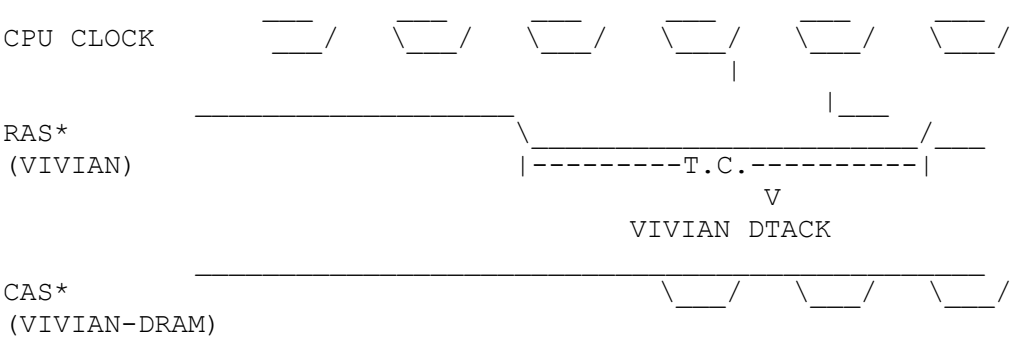
4.6 DRAM CONTROL

The refresh counter is external to Vivian and is multiplexed onto the DRAM address lines during refresh. The RFSH line of VIVIAN is used to control the multiplexing of the refresh counter onto the DRAM address bus and enables the refresh counter to be toggled by RAS* during the refresh mode. CAS* is the multiplex signal to select the row address and the column address, and DCAS* signal is used to latch the column address.

4.7 PHYSICAL BLOCK CONTROL

1. Unidirectionl-synchronous:

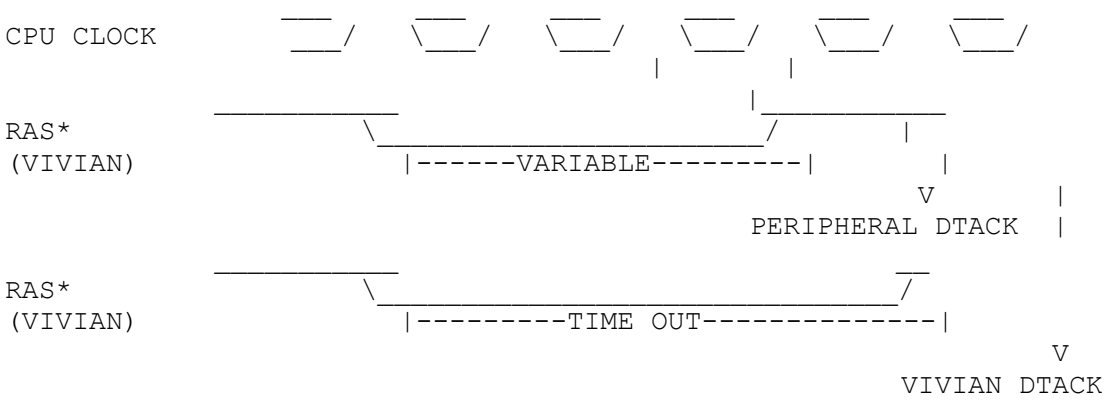
This is the normal chip select with length of the RAS*-CAS* being selected by the timing attribute.



2. Unidirectional-asynchronous:

This chip select is used with a slow or an asynchronous peripheral. The peripheral device must have its own DTACK* to terminate the chip select. VIVIAN deselects the RAS* as soon

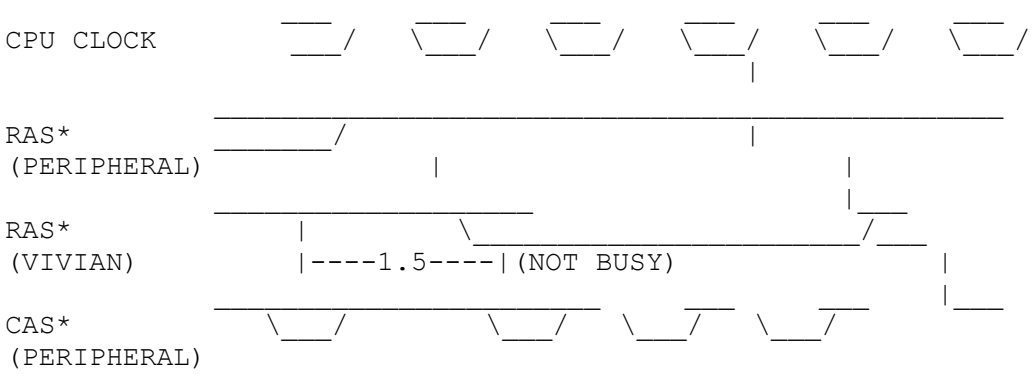
as the external DTACK* is detected. VIVIAN has a time out after which it deselects the peripheral and send its own DTACK*.



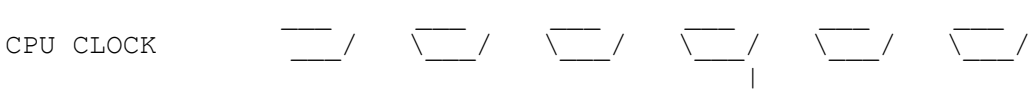
3. Bidirectional-synchronous

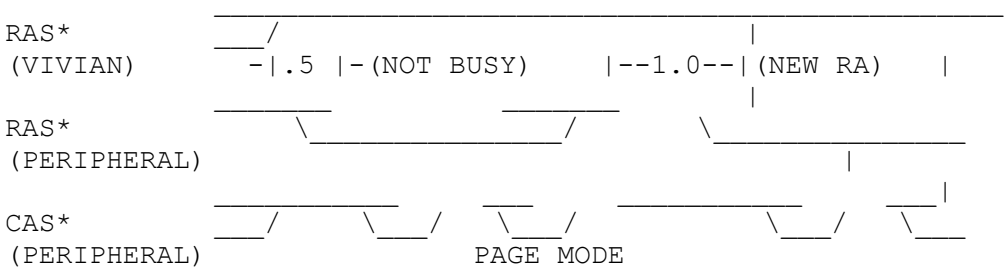
If the physical block address is overlayed between the CPU and another device, i.e. sprite generator that accesses a graphic DRAM, then the arbitration between CPU and the second device is handled by Vivian which gives the second device a priority over the CPU. Vivian generates RAS* on the rising edge of the system clock. All other device that assert RAS* must generate RAS* on the falling edge of the system clock. The priority is established by the fact that Vivian can not reassert RAS* until one-and-a-half clock after an external RAS*, whereas external RAS* can be asserted only a half clock after a Vivian RAS*.

VIVIAN INITIATED TRANSFER



PERIPHERAL INITIATED TRANSFER

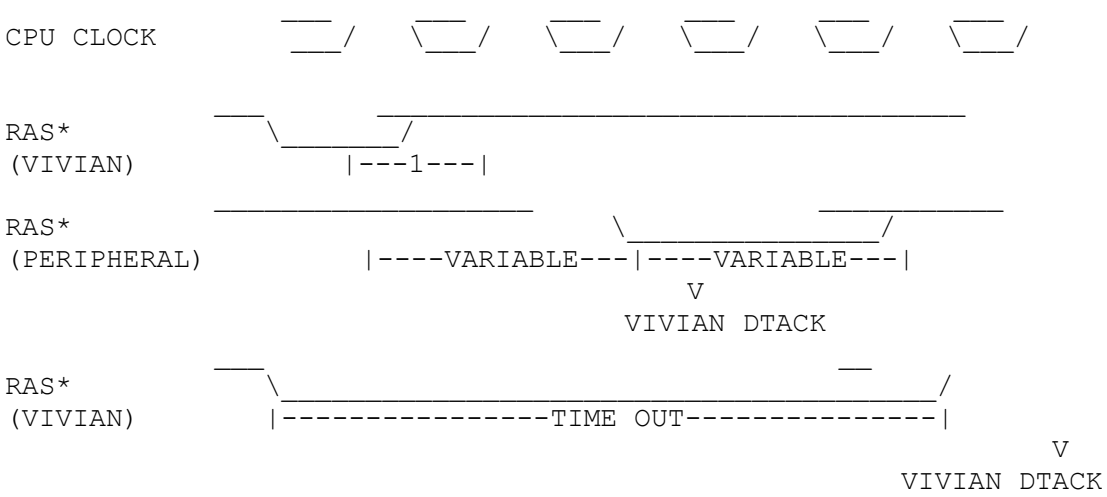




PERIPHERAL AUTOMATICALLY CHANGES THE CAS* TIMING FROM NEGATIVE CLOCK TO POSITIVE CLOCK AS SYSTEM SWITCHES FROM VIVIAN TO THE PERIPHERAL.

????? 4. Bidirectional asynchronous:(Handshake)

This chip select is the standard asynchronous handshaking protocol. VIVIAN has a time out after which it deselects the peripheral and send its own DTACK*.



(THIS SECTION WILL BE COMPLETED ONCE THE CHARACTERIZATION IS IN)

5. ELECTRICAL SPECIFICATION

5.1 MAXIMUM RATINGS

Supply Voltage
Input Voltage
Operating Temprature Range
Storage Temprature

5.2 DC ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Units
Input High Voltage				
Input Low Voltage				
Input Leakage Current				
Output High Voltage				
Output Low Voltage				
Power Dissipation				
Capacitance				

5.3 AC ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Units
Clock Period				
Clock Width Low				
Clock Width High				
Clock Fall Time				
Clock Rise Time				
.				
.				
ETC				

6. COMPATIBILITY

6.1 NS 16000

The MC68010 signals that connects to Vivian are:

AD14-AD23	Output
DAT0-DAT3	Output
AS*	Output
DS*	Output
DTACK	Input
R/W*	Output

The equivalent connectin to NS16032 are:

AD16-A23,AD14,AD15	Output
AD0-AD3	Output
ADS*	Output
DS*/FLT*	Output
RDY	Input
DDIN*	Output

6.2 AMY SOUND GENERATION SYSTEM

AMY sound generation system consists of AMY sound generator chip, 6809 CPU, and RAM. In order to use the AMY RAM as part of the physical block addressed by Vivian it is necessary to disable the address and data bus of the AMY CPU.

7. DESIGN OPTIONS

7.1 ASSOCIATIVE ARRAY

The associative array is designed for maximum of 16 chip select outputs. Each chip select consists of 80 gates. One can reduce the number of chip selects to minimum of 8.

7.2 MASKED ADDRESS

The mask registers requires 50 gates for each chip select if a 10 bit latch per line is used to mask out indivisual bits. One way to reduce the number of gates is to have a smaller number of bits that could be masked. Another approach would be to have one latch that masks a fixed number of bits, or multiple latches with each controlling different size masks.

7.3 TIMING/CONFIGURATION REGISTERS

The timing and configuration registers require 100 gates for each chip select if 10 bit latch per line is used for each of the attributes. Each of the attributes can be confortably be reduced to 4 bits which would require 40 gates.

7.4 TIMING GENERATORS

There are several options on the timing generation. HSYNCH and DS* may be internally generated, and DCAS* may be externally generated. Net result is saving of three pins.

7.5 REFRESH

Instead of having an external refresh counter one might want to add the refresh on board VIVIAN in which case there

will be 7 additional pins.

7.6 GATE COUNT (ONLY FOR THE REGISTERS)

16 CHIP SELECTS/10 BIT ATTRIBUTE/10 BIT MASK	3680
16 CHIP SELECTS/ 4 BIT ATTRIBUTE/10 BIT MASK	2720
16 CHIP SELECTS/ 4 BIT ATTRIBUTE/ 1 BIT MASK	2000
8 CHIP SELECTS/10 BIT ATTRIBUTES/10 BIT MASK	1840
8 CHIP SELECTS/ 4 BIT ATTRIBUTES/10 BIT MASK	1360
8 CHIP SELECTS/ 4 BIT ATTRIBUTES/ 1 BIT MASK	1000

EACH CHIP SELECT	80 GATES
EACH ATTRIBUTE BIT/CHIP SELECT	10 GATES
EACH MASK BIT/CHIP SELECT	5 GATES